Interactions effects in weakly confined quasi one-dimensional quantum wire

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A thesis submitted for the degree of

Doctor of Philosophy

October 2016

Declaration

I, Henry Edward William Montagu confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Acknowledgements

First and foremost, I would like to thank Prof. Sir Michael Pepper for his supervision. This work would not have been possible without his continuous and invaluable support and encouragement. There are no sufficient words that express my indebtedness and gratitude towards him. I would like to deeply thank my second supervisor Dr. Sanjeev Kumar who gave up his lot of valuable time to supervise and guide me throughout the Ph.D. In addition, I would like to thank Dr. Ian Farrer and Prof. Dave Ritchie for growing high-quality wafers which I used to fabricate devices for my Ph.D. work. Also I thank Prof. Chris Ford for his data acquisition software, CryoMeas. I am grateful to all the members of our research group who have helped in many ways throughout this Ph.D. Finally, I would like to thank my family and friends for their support and help throughout the Ph.D.

Abstract

Since the initial realisation of split-gate device and quantised plateaus of conductance in one-dimensional quantum wires, there has been immense interest in studying transport through one-dimensional electron systems to investigate many-body effects. This thesis contains results of experiments performed on novel discrete quantum devices with potential for tuning the confinement as well as the electron density to investigate many-body effects and electron-electron interactions in weakly confinement quantum wires. This thesis covers a detailed development of technology for fabricating novel discrete quantum devices consisting of mid-line, top and back gates patterned along with standard split-gates devices. A novel mid-line gated, split gates device demonstrates the possibility of creation of two lateral one-dimensional quantum wires in a single two-dimensional electron gas (2DEG). This allows the systematic investigation of interaction effects between the quantum wires. Several measurements are performed to further characterise such laterally created quantum wires system in detail. It is also shown that the two one-dimensional quantum wires created out of a single 2DEG exhibit finite coupling between them as a function of mid-line gate thickness. This coupling manifested itself through crossing and anti-crossing of the subbands.

The thesis also covers experimental investigations performed on a weakly con-

fined, low-density quasi-one-dimensional system which was achieved by developing novel back-gated split-gate devices. The thesis presents the possible experimental evidence of two interaction phenomena which occur in the low-density regime such as spontaneous spin polarisation and spin-incoherent transport in one-dimensional quantum wires. The experimental evidence of spin-incoherent transport can be seen in the form of a conductance plateau at $0.5(2e^2/h)$ at very low electron density, whereas the spontaneous spin polarisation shows an additional plateau at $0.5(2e^2/h)$ along with plateau $(2e^2/h)$.

The experimental results presented in the thesis give an important insight and advances in the research of many-body physics in one-dimensional quantum wires.

Publications

Montagu H, Kumar S, Farrer I, Ritchie D, Pepper M *"Wave function Mixing in horizontally aligned One-dimensional wire "*, Physical Review B (2016): In Preparation.

Montagu H, Kumar S, Farrer I, Ritchie D, Pepper M (2016) *"Observation of spin-Incoherent behavior in the ground state of interacting one-dimensional electrons"*, Journal of Applied Physics Letters (2016): In Preparation.

Contents

List of Figures

List of Tables

Acronyms

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$1D$	One-dimension
$2D$	Two-dimension
$2DEG$	Two-dimensional electron gas
AC	Alternating current
DC	Direct current
EBL	Electron-beam lithography
$GPIB$	General-purpose interface bus
$HEMT$	High electron mobility transistor
IPA	Isopropyl alcohol
LED	Light-emitting diode
MBE	Molecular beam epitaxy
$MIBK$	Methyl-isobutyl ketone
$MOSFET$	Metal-oxide-field-effect-transistor
$PMMA$	Poly-methyl-meth-acrylate
QPC	Quantum point contact

SEM	Scanning electron microscope
ZBA	Zero-bias anomaly

Chapter 1

Introduction

1.1 Preface

Over the last 50 years, the tremendous progress of miniaturisation of electronic devices has been achieved thanks to the technological evolution in device fabrication. The main challenge is that when devices are scaled down, the assumptions of the conventional transport theory are no longer valid about length and energy scales. When the size of the device is comparable to the mean free path of electrons, the device is in the regime of mesoscopic transport. New and novel effects happen in that regime which give rise to a new science and profoundly change the device performance. This encouraged a huge interest in researching mesoscopic physics which can possibly hold significance to the advances in nanotechnology. The prefix "meso" comes from the Greek word means "in between" or "intermediate". The mesoscopic system refers to a system that lies in between a macroscopic system, which can be described by classical physics and the microscopic system, which is described by quantum physics. Industrial technological advances have established new materials of unprecedented quality and high-resolution processing techniques which made the realisation of lower-dimensional devices possible.

The properties of low-dimensional systems are often of remarkable interest both for fundamental physics and practical applications. At low temperatures, the classical explanation of electron transport in lower-dimensional devices fail as

quantum phenomena dominates leading to fundamental changes in the transport and electronic properties of semiconductor devices.

1.2 Mesoscopic Transport

The criteria for a mesoscopic system is that the device size must be smaller than or comparable to the electronic mean free path. The de-Broglie wavelength of electrons at the Fermi edge is defined as

$$\lambda_F = \frac{h}{\sqrt{2m^* E_F}} \tag{1.1}$$

where m^* denotes the effective electron mass and E_F is the Fermi energy. If the feature size of the device is comparable to de-Broglie wavelength, the electrons will pass ballistically through the constriction and the kinetic energy of the electrons will be quantised.

If size quantisation takes place in one spatial direction only i.e. restrict the motion of electron in one direction, the electron system is confined to two dimensions forming two-dimensional plane of electrons. If electrons are confined in a two spatial direction, then the electron transport becomes one-dimensional, and it is called a quantum wire. If the electrons are confined in three directions, the electron transport becomes zero-dimensional and it is called a quantum dot.

1.2.1 Fermi Wavelength

The Fermi wavelength of electrons, $\lambda_F = 2\pi/k_F$, is the de-Broglie wavelength of the electron at the Fermi edge. Quantisation happens when the sample length

is comparable to the Fermi wavelength. In a GaAs/$Al_xGa_{1-x}As$ semiconductor heterostructure, the Fermi wavelength of the electron can be as big as 100 nm, and thus can be comparable to the size of the device. The Fermi wavelength is inversely proportional to the electron density n_d where d is the dimension of the electron transport. Taking into account the spin degeneracy of electron which is 2 for GaAs and using the effective mass approximation, the Fermi wavelength can be expressed as

$$3D: \qquad \lambda_F = 2^{\frac{3}{2}} \sqrt[n]{\frac{\pi}{3n_3}} \tag{1.2}$$

$$2D: \qquad \lambda_F = \frac{\sqrt{2\pi}}{n_2} \tag{1.3}$$

$$1D: \qquad \lambda_F = \frac{4}{n_1} \tag{1.4}$$

Thus, the Fermi wavelength can be calculated if the electron density is known and the electron density can be obtained using the Quantum Hall measurements.

1.3 Low Temperature Measurements

Devices have been fabricated using GaAs and $Al_xGa_{1-x}As$ heterostructures and for a device to show quantum transport, it has to be cooled down below 4.2 K.

However, some devices pushed the temperatures limit of quantisation in GaAs/$Al_xGa_{1-x}As$ heterostructures to around 40 K [6–8]. GaAs/$Al_xGa_{1-x}As$ heterostructures have been used extensively in research of mesoscopic transport. The two-dimensional electron gas in GaAs heterostructures can have a superior quality and ultra-high mobility. The electron mean free path can exceed 120 μm at low temperatures [9]. A technique called modulation doping laid the foundations for achieving ultra-high electron mobilities which reduced scattering significantly [10, 11].

The samples are cooled down because phonons and accusation scatterings are major difficulty for electrons as it reduces greatly the mean free path of electrons at room temperature. Optical phonons have energies around 36 meV and are frozen out below about 30 K thus their effect is reduced by cooling down the samples. Smaller feature sizes lead to stronger size quantisation and larger separation between subband energy levels. Another advantage of cooling down the device is reducing thermal smearing, quantised plateaus are visible when the thermal smearing of the Fermi function becomes small compared to the energy level spacing.

1.3.1 Ballistic Transport

For a device to exhibit ballistic transport, electrons have to pass from one lead to the another without scattering and the mean free path L_e is comparable or smaller than sample length L. The mean free path is defined as the average distance an electron travels before being scattered by large-angle scattering events like impurity or electron-phonon interaction.

1.4 Two Dimensional Electron Gas

Electrons can be confined within an interface between two different materials. A two dimensional electron gas (2DEG) can be created by confining electrons within an interface between a semiconductor and an insulator such as Si MOSFET (Metal Oxide Semiconductor Field Effect Transistor) which was used to realise the first 1D devices [12, 13]. GaAs/$Al_xGa_{1-x}As$ heterostructures soon dominated the research field of one dimensional devices. In 1979, Störmer *et al.* had experimentally grown the first modulation-doped heterostructure using GaAs/$Al_xGa_{1-x}As$ based on an idea proposed by Dingle *et al.* which laid the foundation of achieving high electron mobilities [10, 11]. The term 'modulation-doped' means that there is a spatial separation of the doped layer from the 2DEG by using a spacer layer in between which greatly reduces the scattering from ionised donors and thus increases the electron mobility.

1.4.1 Wafer Growth

GaAs/$Al_xGa_{1-x}As$ high electron mobility transistors (HEMT) are grown using Molecular Beam Epitaxy (MBE) technique. The subscript x refers to the mole composition of aluminium which is present in $Al_xGa_{1-x}As$ which is usually 0.33 in wafers used in this thesis. MBE growth is a sophisticated process where materials inside the effusion cells are vaporised and directed at a heated substrate under ultra high vacuum. The quality of the wafer grown is determined by the defects and impurities inside the wafer. Impurities are reduced during growth by using clean sources and extensively cleaning the MBE chamber and for growth to occur under ultra-high vacuum. Defects occur due to lattice strain caused by displaced

atoms within the crystal lattice. A mismatch in the lattice constants between two materials can lead to strain or dislocations within the crystal structure at the interface and thus it is not desirable to have the 2DEG near the interface. $Al_xGa_{1-x}As$ is favoured to be used with GaAs as both materials have similar lattice constants and very smooth interfaces can be grown on top of one another.

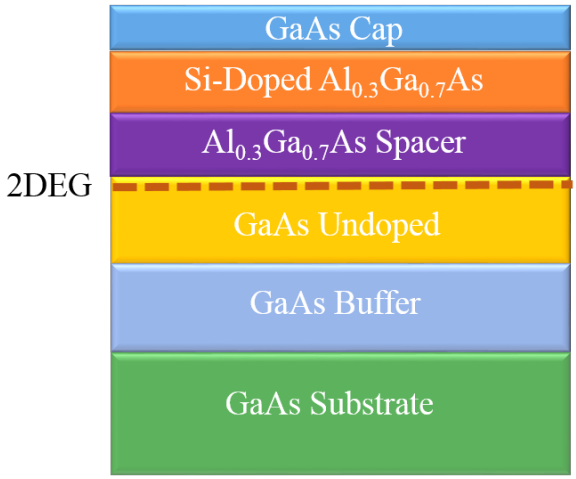

Figure 1.1: A schematic diagram of the layers of a typical GaAs wafer grown using MBE where the 2DEG is formed at the interface of GaAs and $Al_xGa_{1-x}As$ spacer layer.

MBE growth happens on a polished semi-insulating GaAs substrate. The substrate is polished to provide a smooth surface. The first grown layer is a thick GaAs buffer layer of 1000 nm thickness to separate the GaAs substrate from the 2DEG. A spacer layer of $Al_xGa_{1-x}As$ is grown to separate the Si donors from the 2DEG to reduce scattering. A layer of Si-doped $Al_xGa_{1-x}As$ is grown where the Si atoms are used for n-doping of GaAs material. A final thin cap layer of GaAs is grown to protect and prevent the oxidisation of $Al_xGa_{1-x}As$ layer. The 2DEG is formed in the GaAs just below GaAs/$Al_xGa_{1-x}As$ interface as indicated in figure 1.1.

1.4.2 2DEG Formation

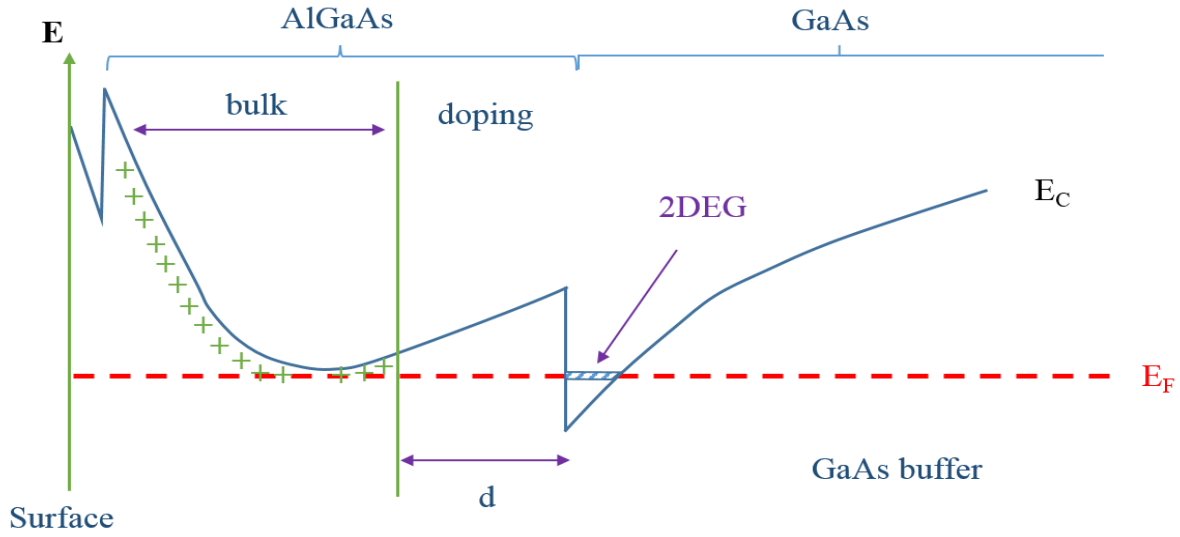

Figure 1.2: A schematic diagram of the conduction band of the GaAs/$Al_xGa_{1-x}As$ heterostructure. Electrons move away from the Si doped $Al_xGa_{1-x}As$ layer leaving behind ionised Si donors which are represented by '+' and d is the distance from the heterostructure interface to the middle point of the depleted region by charge transfer. Graph is adapted from Ref [1].

The 2DEG forms in a GaAs HEMT due to difference in the energy band gap between GaAs and $Al_xGa_{1-x}As$. The size of such a band gap can be controlled by changing the mole fraction of Al, x in the $Al_xGa_{1-x}As$ layer. Electrons are supplied by the Si dopants in the $Al_xGa_{1-x}As$ layer and at room temperature, the electrons can move around and are thermally activated over the small barrier in the conduction band into the GaAs conduction band. At low temperatures, the electrons have lower energy and get trapped in a triangular quantum well at the GaAs/$Al_xGa_{1-x}As$ interface. The triangular potential quantum well is created due to the mismatch in the band gap between the GaAs and $Al_xGa_{1-x}As$ layers as shown in figure 1.2. The electrons are free to move in the x-y plane at

the interface however motion is restricted in the z-direction which results in the creation of a two-dimensional sea of electrons.

1.4.3 Illumination

The illumination of $Al_xGa_{1-x}As$ is capable of changing the density of the 2DEG and can be achieved by using a red LED. The presence of Si donors in the $Al_xGa_{1-x}As$ layer gives rise to DX centres. The light is capable of exciting electrons out of the DX centres to the 2DEG and the electrons are then trapped in the potential well and higher density is achieved. Thus, controlled illumination can produce a variety of electron densities and mobilities in the device.

1.5 Split-Gates Devices

The motion of electrons can be further restricted in a 2D system to create a 1D system and the 1D devices can be realised using a 'split-gates' where a pair of metallic split-gates are deposited on the top of the surface of a $GaAs/Al_xGa_{1-x}As$ heterostructure. The 2DEG beneath the split-gates is depleted when a negative voltage is applied which allows electrons to move in a narrow constriction between the two reservoirs in the 2DEG. The width of the 1D constriction can be tuned by the voltage applied to the split-gates; smaller split-gates devices are usually referred to as quantum point contact (QPC).

In 1986, Thornton *et al.* developed the first 1D devices using a pair of split-gates [14]. In 1988, Wharam *et al.* [15] and van Wees *et al.* [16] measured the first 1D devices using split-gates where quantised conductance in steps of $2e^2/h$ was observed and the measurement was done by ramping the spilt-gate voltage

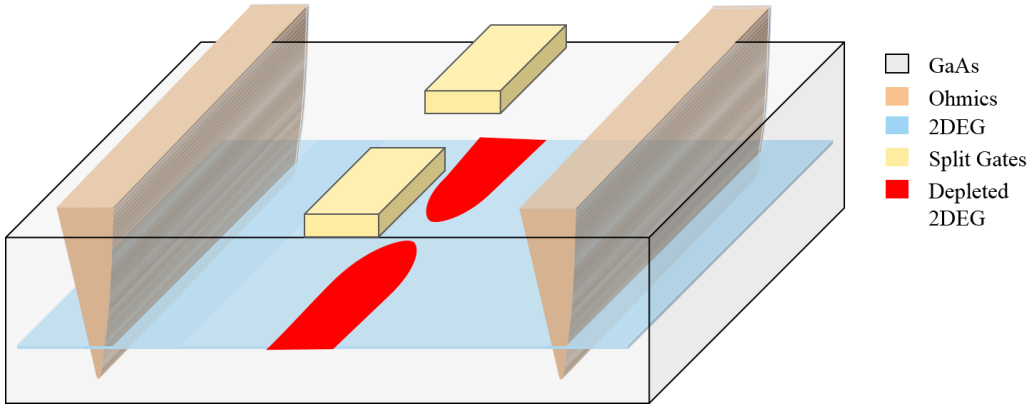

Figure 1.3: A schematic diagram of a device which contains a pair of split-gates deposited on a GaAs heterostructure. A negative voltage is applied to the split-gates where electrons below in the 2DEG is depleted which leaves a narrow constriction.

which changes the width of the channel and thus the number of occupied 1D subbands below the Fermi energy. The conductance was measured as a function of split-gates voltage and showed a series of quantised steps in units of $2e^2/h$.

Figure 1.4 shows the quantised conductance of a 1D constriction using a pair of split-gates. Figure 1.4 a) shows a drop in conductance as the electrons start to get depleted underneath the split-gates. The gradient of the conductance trace changes dramatically which indicates the definition of a quasi-1D constriction in the 2DEG. The graph shows a series of steps until the conductance drops to zero where no more electrons can flow through the constriction. The conductance trace includes the resistance contributions from different components in series with the 1D constriction. The actual conductance through the 1D constriction is calculated by removing the series resistance (2.0 kΩ). Figure 1.4 b) shows the corrected conductance data where the series resistance is removed and the plateaus are quantised units of $2e^2/h$.

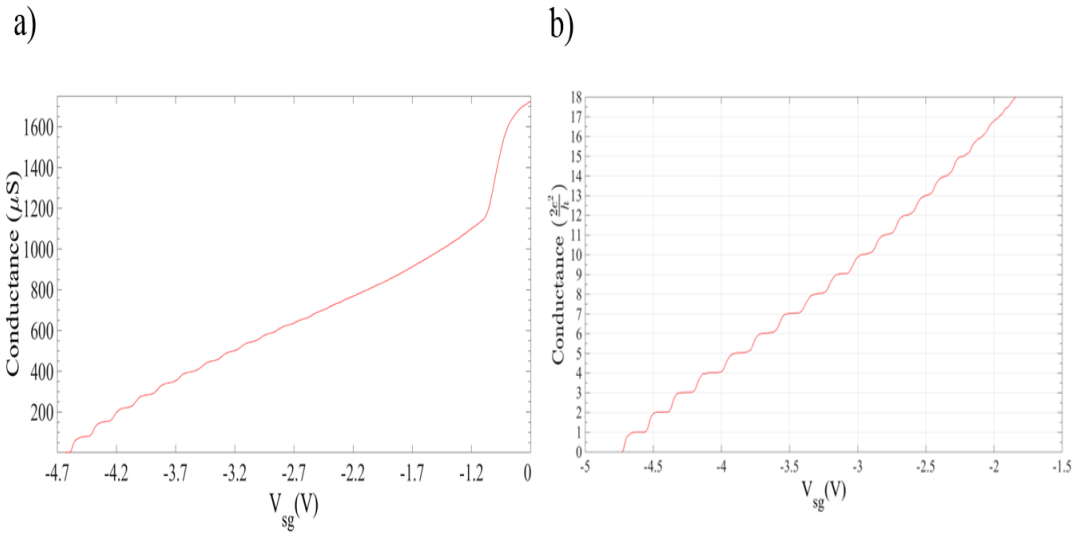

Figure 1.4: a) Conductance trace as a function of split-gate voltage ,V_{sg}, of a split-gates device. Figure 1.4 b) shows the conductance trace as a function of split-gate voltage ,V_{sg}, where the series resistance has been removed.

1.5.1 Device Design

The split-gates devices remain the dominate method to explore 1D systems however they are limited in exploring different density regimes and the addition of new novel gates enhances the versatility of the split-gates device [17–19]. The electron density of the 1D quantum wire can be independently controlled by the addition of an extra gate to the split-gates device. These extra gates can be placed either on the front or the back of the device and there are various possibilities for where the extra gate can be placed. Figure 1.5 shows the experimental realisation of a mid-line, top and back gates to control the carrier density in the channel.

1. A mid-line gate

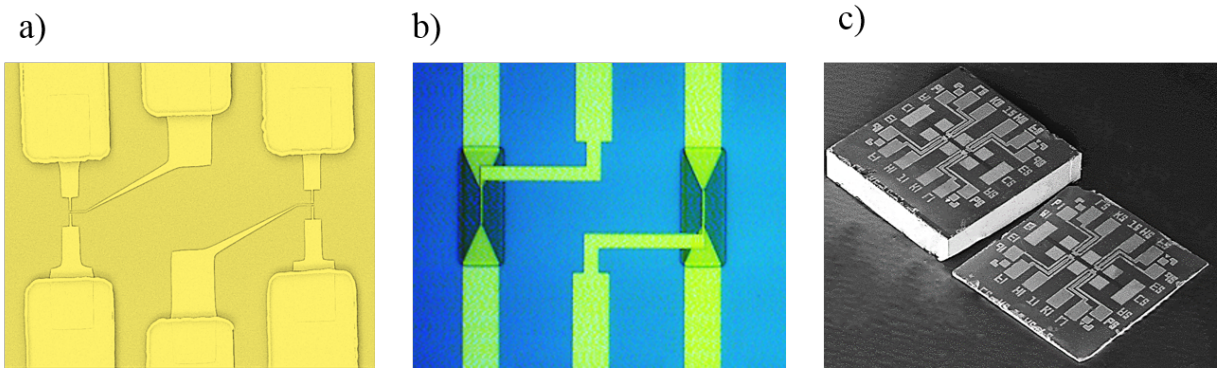

Figure 1.5: a) shows split-gates device with a mid-line gate b) shows a split-gates device with a top gate c) shows a chip of height 550 μm containing split-gates devices (left); and on the right a chip thinned down to 50 μm is shown. Metallisation is done on the back of the device for back gate electrode purpose.

2. A top gate

3. A back gate

A mid-line gate would lie on the surface of the wafer between the split-gates and is along the transport direction which is shown in Figure 1.5 (a). It is easier to add a mid-line gate as the patterning and metallisation of the gate happens at the same time with the split-gates. By applying a negative potential to the gate, electrons are repelled from the 2DEG thus changing the density in the centre of the channel. The mid-line gate can introduce asymmetry in the channel as one side of the channel may be depleting before the other.

The top gate can be formed on top of the split-gates by deposing an insulating dielectric in between which is shown in Figure 1.5 (b). The top gate lies above the split-gates and can be used to vary the carrier density of the 1D quantum wire. The top gate requires two additional e-beam fabrication stages; one for the dielectric deposition and another for the top gate metallisation.

The back gate device is used to vary the 2D carrier density where the device is thinned and a gate is deposited on the back of the device however it adds complexity to the fabrication process and the device may become fragile (Figure 1.5 (c)). An overall back gate will deplete the entire 2DEG and therefore the 2D resistance will increase as the back gate is made more negative. However, this back gated technique was found to be very effective in studying interaction effects in 1D quantum wires.

1.6 Alternative 1D systems

Different fabrication methods have been used to realise 1D systems such as top down fabrication to create nano-wires or bottom up fabrication to create carbon nano-tubes however the device characteristics are poor due to induced damage by fabrication and poor lateral control [20, 21]. Other fabrication techniques were deployed to create 1D constriction like wet etching techniques [22–24], cleaved-edge overgrowth [25], focused ion beam implantation [26, 27], and gates patterning using a metallic AFM tip to oxidise the surface of the semiconductor [28, 29]. These fabrication techniques create strongly confined 1D quantum wires with a large subband spacing compared to GaAs/$Al_xGa_{1-x}As$ split-gates devices and thus, quantised conductance was observed at higher temperatures up to 30 K [23]. On the other hand, these devices tend to be more complicated to fabricate and moreover less clean due to disorder within the channel and scattering from the boundaries of the channel. The relative ease of fabricating split-gates devices and higher quality with GaAs/GaAs/$Al_xGa_{1-x}As$ material systems ensured a clear observation of quantised plateaus. This has therefore made the split-gates

technique as the most popular technique to realise 1D devices.

1.7 Outline of the Thesis

In this chapter an introduction to the field of 1D transport has been presented which includes the experimental realisation of 1D transport using split-gates devices. Chapter 2 explores further background theory in 1D transport which is relevant to the work in this thesis. Chapter 3 presents the low-temperature equipment and measurement techniques used to obtain the data presented in the thesis. Chapter 4 presents the fabrication processes for devices used for measurements in this thesis and the optimisation of NiAuGe Ohmic contacts. The experimental data are presented in chapters 5 and 6. Chapter 5 presents measurements using novel mid-line gated split-gates devices in which the two laterally positioned 1D wires were attempted to be created in a single 2DEG and manipulating the wave function mixing. Chapter 6 presents the two coupled one dimensional wires where crossing and anti-crossing of the subbands occur and a section on the back gated split-gates devices has been presented. In the last chapter 7, conclusions from the two experimental chapters are presented and also future work is suggested.

Chapter 2

Theoretical Review of 1D Quantum Transport

2.1 Electron Transport in Metals

Transport of electrons in metals can be described using the Drude model which was proposed by Paul Drude in 1900 [30, 31]. The conductance G can be defined as

$$G = \frac{\sigma A}{L} \tag{2.1}$$

where A is the cross section of the metal, σ is the Drude conductivity and L is the length of the metal. The Drude conductivity can be expressed as

$$\sigma = e n_e \mu = \frac{n_e e^2 \tau}{m_e} \tag{2.2}$$

where e is electron charge, μ is the electron mobility, n_e is the density of electrons, L is the average free time before electrons are scattered. The Drude model can describe the diffusive transport of electrons since electrons collide many

times and at random through the metal. However, the Drude model fails to describe electron transport in a one-dimensional wire since there is no scattering between electrons as the size of the 1D constriction is much smaller than the mean free path of electrons and electron is in ballistic transport regime. A model to describe the behaviour of electrons in 1D wires was needed like Landauer-Büttiker model.

2.2 Density of States

The density of states is a crucial aspect of an electron system as it determines the transport properties of the system. The density of states depends on the dimensionality of system. The density of states is defined as the number of available eigenstates in a given energy space from E to $E + dE$ per unit volume.

$$D_n(E) = \frac{d\Omega_n(E)}{dE} \tag{2.3}$$

where Ω is the energy carrier probability density. For 3D bulk density, the probability density of state $g(k)$ with units of probability per unit k

$$g(E) = g(k)\frac{dk}{dE} \tag{2.4}$$

Given that

$$k = \sqrt{\frac{2m^*E}{\hbar^2}} \quad and \quad \frac{dk}{dE} = \frac{1}{2}\sqrt{\frac{2m^*}{\hbar^2}}\frac{1}{\sqrt{E}} \tag{2.5}$$

thus

$$g_3(E) = \frac{k^2}{\pi^2}L^3\frac{dk}{dE} = \frac{L^3}{2\pi^2}\left(\frac{2m^*}{\hbar^2}\right)\sqrt{E} \tag{2.6}$$

Dividing the result of the equation above by the real space volume L^3, the density of states in bulk semiconductor

$$D_3(E) = \frac{1}{2\pi^2}\left(\frac{2m^*}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E} \tag{2.7}$$

For 2D dimensional systems, the probability density per unit k can be expressed as

$$g(k) = \left(\frac{k}{\pi}\right)L^2 \tag{2.8}$$

and substituting the result above in equation (2.4) and (2.5)

$$g_2(E) = \left(\frac{m^*}{\pi\hbar^2}\right)L^2 \tag{2.9}$$

and the density of states for 2D systems can be expressed as

$$D_2(E) = \frac{g(E)}{L^2} = \left(\frac{m^*}{\pi\hbar^2}\right) \tag{2.10}$$

For 1D dimensional systems, the probability density per unit k can be expressed as

$$g(k) = \frac{L}{\pi} \tag{2.11}$$

and substituting the result above in equation (2.4) and (2.5)

$$g_1(E) = \frac{L}{2\pi}\sqrt{\frac{2m^*}{\hbar}}\frac{1}{\sqrt{E}} \tag{2.12}$$

and the density of states for 1D systems can be expressed as

$$D_1(E) = \frac{2g(E)}{L} = \frac{1}{\pi}\sqrt{\frac{2m^*}{\hbar^2}}\frac{1}{\sqrt{E}} \tag{2.13}$$

Figure 2.1 shows the density of states of semiconductor with 3, 2, 1 and 0 degrees of freedom for electron transportation. Systems with 2, 1 and 0 degrees of freedom are called quantum well, quantum wires and quantum dots respectively. Table I summarizes the equations of density of states, dispersion relation and Fermi wavelength for 3, 2 and 1 degrees of freedom.

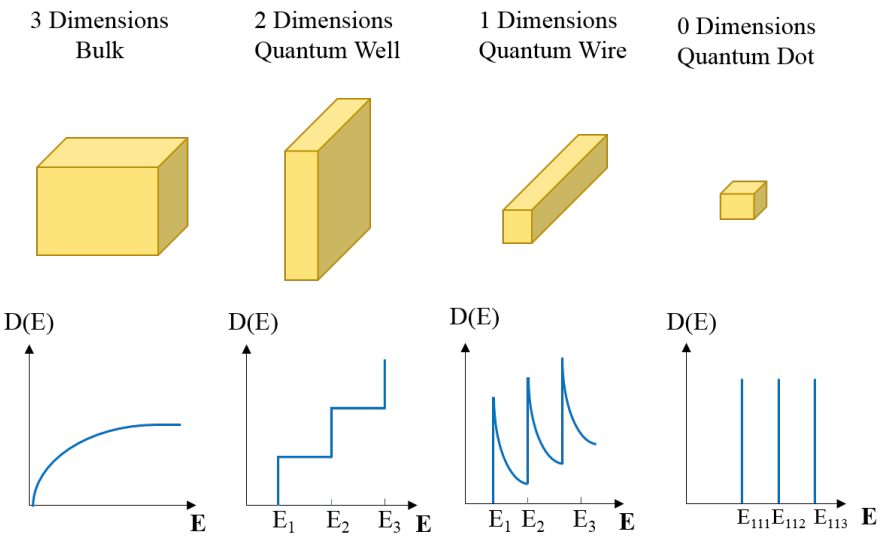

Figure 2.1: Schematic diagram of density of states, D(E), as a function of energy, E, for different degree of freedom of dimensions.

Degrees of freedom	Dispersion (kinetic energy)	Fermi Wavelength, λ_F	Density of states, D(E)
3 (Bulk)	$E = \frac{\hbar^2}{2m^*}(k_x^2 + k_y^2 + k_z^2)$	$\lambda_F = 2^{\frac{3}{2}} \sqrt[n]{\frac{\pi}{3n_3}}$	$D_3(E) = \frac{1}{2\pi^2}\left(\frac{2m^*}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E}$
2 (Quantum Well)	$E = \frac{\hbar^2}{2m^*}(k_x^2 + k_y^2)$	$\lambda_F = \frac{\sqrt{2\pi}}{n_2}$	$D_2(E) = \frac{g(E)}{L^2} = \left(\frac{m^*}{\pi\hbar^2}\right)$
1 (Quantum Wire)	$E = \frac{\hbar^2}{2m^*}(k_x^2)$	$\lambda_F = \frac{4}{n_1}$	$D_1(E) = \frac{2g(E)}{L} = \frac{1}{\pi}\sqrt{\frac{2m^*}{\hbar^2}}\frac{1}{\sqrt{E}}$

Table I: shows the density of states for semiconductor with 3, 2 and 1 degrees of freedom for the prorogation of electrons. The dispersion relations are assumed to be parabolic.

2.3 Quantisation of Conductance in 1D system

A simplified derivation in a perfect 1D channel where subbands are non-interacting and will not scatter. Consider the current due to single 1D sub-band labelled i between two perfect leads [15, 32]

$$I_i = ne\delta v \tag{2.14}$$

where n is the number of carriers per unit length in the subband, e is the charge of electron, δv is the increase in electron velocity acquired on passing through the 1D constriction. The density of states in 1D wire $D_n(E)$ as function of energy is given by

$$g_1(E) = \frac{g_s}{2\pi\hbar}\sqrt{\frac{2m^*}{\hbar}}\frac{1}{\sqrt{E}} \tag{2.15}$$

where g_s is the spin degeneracy, and m^* is the effective mass. Integrating to obtain the number of carriers gives

$$n = \int_0^{E_F} N(E)dE = \frac{g_s}{\pi\hbar}\left(\sqrt{\frac{m^*E_F}{2}}\right) = \frac{g_s m^* v_F}{2\pi\hbar} \tag{2.16}$$

where E_F is the Fermi energy and v_F the corresponding Fermi velocity. Obtaining v_F as a function of the applied voltage V

$$eV = m^* v_F \delta v + \frac{1}{2}(v_F)\delta v^2 \tag{2.17}$$

For the case $v_F \ll v_F$, the increase in velocity is given by

$$\delta v = \frac{eV}{m^* v_F} \tag{2.18}$$

Substituting equations (2.16) and (2.18) into equation (2.14) gives

$$I_i = \frac{g_s e^2 V}{2\pi\hbar} \tag{2.19}$$

The conductance , $G = I/V$, can be expressed as

$$G_i = \frac{2e^2}{h} \tag{2.20}$$

where G_i is the conductance from a single sub-band and $g_s = 2$ for electrons. Assuming that subbands are non-interacting and will not scatter, the total conductance is given by

$$G = \sum_{N}^{m} G_i = \frac{2e^2}{h} N \tag{2.21}$$

where the summation is over all N occupied subbands.

2.3.1 The Landauer-Büttiker Formalism

Landauer had showed in 1957 that conductance of an ideal conductor can be expressed as a function of the transmission and reflection probabilities at a

barrier[33, 34]. In the last section, it was assumed that a perfect 1D conductor was used as there were no constrictions or a potential barrier between the drain and source reservoirs. In an actual 1D device, the electrostatic potential confining generated by split-gates and the potential in the 2DEG varies smoothly as a function of position. Later, Büttiker had presented a model of the conductance of a system which contains ideal leads. He assumed that the leads are weakly coupled to the reservoir and therefore the potential considered are those of the leads, μ_s and μ_d [35].

$$G = \frac{2e^2}{h}\frac{T}{R} \tag{2.22}$$

where T is transmission coefficient, μ_s and μ_d are the chemical potentials of the electrons in reservoirs and R is the reflection coefficients. In a perfect transmission T = 1 and R = 0, the conductance becomes to infinity. However, Imry had modified the Landauer formula so that the chemical potentials μ_s and μ_d of the electrons in the reservoirs are actually measured [36].

$$G = \frac{I}{\mu_S - \mu_D} = \frac{2e^2}{h}T \tag{2.23}$$

Hence, the conductance remains finite even for a perfect transmission T=1. The finite conductance is considered to be the sum of two contact resistances which exist between each of the 1D leads and the reservoirs to which they are connected.

2.4 Confinement Potential in 1D

The most simple model to describe the potential of the 1D confinement by split-gates is the a parabolic or square well. The Schröedinger equation describing the electrons can described as

$$-\frac{\hbar^2}{2m}\frac{d^2\Psi}{dx^2} + V(x)\Psi(x) = E\Psi(x) \tag{2.24}$$

where $V(x)$ is the confining potential $V(x)$ along the x-direction. For a square well with width L, the confining potential can be expressed as

$$V(x) = \begin{cases} 0 & |x < L| \\ \infty & |x > L| \end{cases} \tag{2.25}$$

Solving the Schröedinger equation, the energy can be expressed as

$$E_n = \frac{h^2 n^2}{8mL^2} \tag{2.26}$$

The confinement potential $V(x)$, for a parabolic well with angular frequency ω that defines the parabola can be expressed as

$$V(x) = \frac{1}{2}m\omega^2 x^2 \tag{2.27}$$

Solving the Schröedinger equation which has a solution in the form of $\Psi(x) =$

$Ce^{(-\alpha x^2/2)}$ where C is dimensionless coefficient, the energy can be expressed as

$$E = (n + \frac{1}{2})\hbar\omega \tag{2.28}$$

Figure 2.2 shows the solution of the wave-functions for 1D harmonic oscillator and the energy levels. The square of the wavefunction indicates the probability of finding the harmonic oscillator.

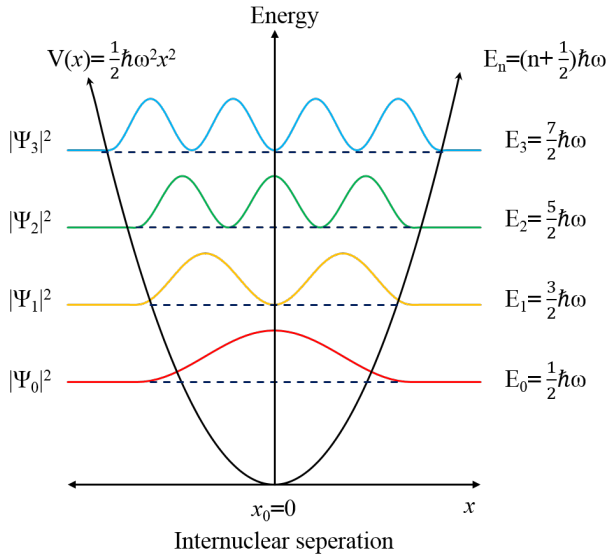

Figure 2.2: A schematic diagram of a parabolic one dimensional potential well with first four allowed energy levels.

The confining potential of 1D system is important as it determines the sub-band energy levels of the system [37–39]. Wharam *et al.* measured the potential in the one dimensional channel in a split-gates device. They reported that a confinement potential where it was flat in the middle and with parabolic walls is more accurate than the parabolic potential [40]. Better models of confinement

were proposed which proposes a smooth and gradual transition of the confinement potential from 2DEG to the 1D system [41].

2.4.1 Saddle Point Approximation

Conductance increases as a step function when the subbands are occupied in an ideal 1D wire. The conductance in a real device increases as smooth monotonic risers and this is the result of quantum tunnelling of electrons and the conductance curve gives an important information about the shape of the potential inside the 1D wire. Büttiker presented an approximation to the potential inside 1D constriction as a saddle-like potential which is given by [42]

$$V(x,y) = V_0 - \frac{1}{2}m^*\omega_x^2 x^2 + \frac{1}{2}m^*\omega_y^2 y^2 \tag{2.29}$$

where V_0 is the electrostatic potential at the saddle point and ω_x and ω_y represents the curvatures of the potential in the x and y directions.

The effective potential can be expressed as a band bottom of the subband in the region of the saddle point and in the absence of quantum tunnelling, the channel has a threshold energy

$$E_n = V_0 - \hbar\omega_y(n + \frac{1}{2}) \tag{2.30}$$

where the channel with energy below the Fermi energy are open, and the channels with energy E above the Fermi energy are closed. Quantum mechanical

tunnelling and reflection introduces partially transmitted modes and the transmission and reflection at the saddle allows for channels which are neither completely open nor closed which permit transmission with a probability function of $T_{n,m}$. The transmission probability $T_{n,m}$ is calculated and can be expressed as [43]

$$T_{n,m} = \delta_{n,m} \frac{1}{1 + e^{-\pi\epsilon_n}} \tag{2.31}$$

and the total conductance is given as a the summation of the transmission probabilities for each mode

$$G = N \frac{e^2}{h} \sum T_{n,m} \tag{2.32}$$

where n and m denote the incoming and outgoing modes. As a consequence, the shape of the saddle-point potential has a significant impact in determining the shape and the quality of the conductance plateaus. For a quantum wire quantisation will not occur if the ratio $\frac{\omega_y}{\omega_x} < 1$ is less than one. When the confinement is symmetric $\frac{\omega_y}{\omega_x} = 1$, plateaus start appearing in the conductance curve and as the ratio increases $\frac{\omega_y}{\omega_x} > 1$, the quality of the plateaus increases and they become longer and flatter.

2.5 1D transport in a Magnetic Field

Applying a magnetic field lifts the spin degeneracy of the 1D subbands, causing additional half integer plateaus to appear in the conductance as multiples of $\frac{e^2}{h}$[15, 44]. When applying a magnetic field, the 1D subbands split by an amount equal to the Zeeman energy, $2\mathrm{g}\mu_\mathrm{b}SB$, where μ_b is the Bohr magneton, g is the Lande g-factor, B is magnetic field and S is the spin angular momentum S=$\frac{1}{2}$.

Applying a magnetic field B changes the Hamiltonian operator and the Hamiltonian is, [45]

$$H = \frac{(\mathbf{P} + e\mathbf{A})^2}{2m^*} + V \tag{2.33}$$

where V is an arbitrary confinement potential, The energy level of the nth 1D subband splits into

$$E_{n,\uparrow} = E_n(B, V) + g\mu_B B/2 \tag{2.34}$$

$$E_{n,\downarrow} = E_n(B, V) - g\mu_B B/2 \tag{2.35}$$

where spin-down is represented by $\downarrow$ which is lower energy subband and spin-up $\uparrow$ subband is represented by $\uparrow$ which is the higher energy subband. $E_n(B, V)$ produces different effects which is dependent on the orientation of the magnetic field. The Landau gauge changes depending on the magnetic field orientation and

gives rise to new effective potentials with contributions from the lateral electrical confinement as well as the magnetic field confinement. There are three magnetic field orientations which are: **B** perpendicular to the plane of the 2DEG, B = (0, 0, Bz), **B** in-plane and parallel to the 2DEG, B = (Bx, 0, 0), and **B** in-plane but perpendicular to the 2DEG, B = (0,By, 0). Titled angles can also be used to examine more complex behaviour where the 2DEG is at angle with the three basic orientations.

2.5.1 Perpendicular Magnetic Field

The application of a perpendicular magnetic does not effect motion in the z-direction which is the axis normal to the 2DEG however it will couple motion in the x-y direction causing electrons to move in cyclotron motion in the plane of the 2DEG. The axis of the quantum wire is along the x-direction and the wire is confined in the y-direction. In the absence of a magnetic field and assuming a parabolic confinement potential for 1D lateral confinement, the 1D energy subbands are expressed as

$$E_{k_x,n} = \frac{\hbar^2 k_x^2}{2m^*} + (n + \frac{1}{2})\hbar\omega_0 \tag{2.36}$$

where ω_0 is the electrical field. Choosing the gauge **A**= $(-By, 0, 0)$ gives rise to an effective potential that includes both lateral electrical confinement and magnetic field confinement and the 1D magneto-electrical subbands can be expressed as [46, 47]

$$E_{k_x,n} = \frac{\hbar^2 k_x^2}{2m_B^*} + (n + \frac{1}{2})\hbar\omega \tag{2.37}$$

where

$$\omega = (\omega_0^2 + \omega_c^2)^{1/2} \quad \text{and} \quad m_B^* = m^*\omega^2/\omega_0^2 \tag{2.38}$$

2.5.2 In-plane Magnetic Field

Applying an in-plane magnetic field causes more complicated effects than the perpendicular magnetic field. The Zeeman splitting occurs independent of the field direction and it lifts the spin degeneracy of the 1D wire.

2.5.2.1 In-plane Magnetic Field Parallel to the Quantum Wire

Assuming a parabolic confinement potential for the 2DEG and 1D confinement, $V(y,z) = \frac{1}{2}\omega_y^2 y^2 + \frac{1}{2}\omega_z^2 z^2$ and using gauge $\mathbf{A}$=(0,$-zB/2$,$yB/2$) for $\mathbf{B}$ = (Bx, 0, 0), the 1D magneto-electrical subbands can be expressed as [45, 46, 48]

$$E_{k_x,m,l} = \frac{\hbar^2 k_x^2}{2m^*} + (l + \frac{1}{2})\hbar\omega_1 + (m + \frac{1}{2})\hbar\omega_2 \tag{2.39}$$

where

$$\omega_{1,2}^2 = \frac{1}{2}(\omega_\parallel^2 + \omega_y^2 + \omega_z^2 \pm \sqrt{(\omega_\parallel^2 + \omega_y^2 + \omega_z^2)^2 - \omega_y^2\omega_z} \tag{2.40}$$

where $\omega_\parallel = eB_\parallel/m^*$ and the energy levels of the electrons are labelled by two

quantum numbers l and m which represents the two confinement directions in the y and z directions. The magnetic field couples the subbands of the 2DEG and 1D constriction into $\hbar\omega_1$ and $\hbar\omega_2$. The subbands energy of the 1D wire $\hbar\omega_1$ decrease as the magnetic field is increased which is called the diamagnetic shift. From equation (2.40), the diamagnetic shift reduces the subband spacing of 1D wire which causes Zeeman crossing at lower magnetic fields [48]. At high magnetic fields, Landau levels will be formed in the 2DEG and 1D subbands will evolve into a Landau level. The term $\hbar\omega_2$ can be neglected in 1D transport.

2.5.2.2 In-plane Magnetic Field Perpendicular to the Quantum Wire

If the magnetic field is perpendicular to axis of the 1D quantum wire and the 2DEG, $\mathbf{B}$ = (0, By, 0) and assuming a parabolic confinement potential for the 2DEG and 1D confinement, the 1D magneto-electrical subbands can be expressed as [48, 49]

$$E_{k_x,m,l} = \frac{\hbar^2 k_x^2}{2m^*(1+(\frac{\omega_c}{\omega_z})^2)} + (l+\frac{1}{2})\hbar\omega_y + (m+\frac{1}{2})\hbar\sqrt{\omega_z^2+\omega_c^2} \tag{2.41}$$

The magnetic field does not change the subband spacing of 1D wire. It should be noted that the effective mass now is magnetic field dependant.

2.6 Non-linear Transport

Transport measurements of 1D systems are usually made in the linear transport regime where the ac voltage applied is an order of magnitude smaller than the energy spacing of the 1D subbands. The measurement performed on the system

should not perturb it. A large dc voltage (source-drain bias) can be applied in addition to the small ac excitation voltage to the sample between the source and drain reservoir. The voltage bias applied across the quantum wire perturbs the electrons in the 1D constriction and interaction effects appear. These non-linear conductance measurements can be used to find the 1D subband spacing.

Glazman and Khaetskii in 1989 explored the non-linear transport regime under finite source-drain voltage and predicted the appearance of half integer plateaus [50]. Kouwenhoven *et al.* experimentally measured the I-V characteristics of quantum point contacts in a non-linear regime [51]. Later, Patel *et al.* observed the appearance of half-integer plateaus in the conductance traces of 1D wires[52, 53]. Martin-Moreno *et al.* presented a theoretical framework for describing the conductance in the non-linear regime of transport defined by a saddle-point potential [54].

Assuming that the dc source-drain bias V_{sd} dropped at the bottleneck of the quantum wire constriction is linear and drops by the amount $\beta e V_{sd}$, the source and the drain chemical potentials can be expressed as

$$\mu_s = E_F + \beta e V_{sd} \tag{2.42}$$

$$\mu_d = E_F - (1-\beta) e V_{sd} \tag{2.43}$$

where E_F is the Fermi energy of the quantum wire and $0 \leq \beta \leq 1$. It is assumed that $\beta = 1/2$ for a symmetric voltage drop across the 1D constriction [50]. The

total current can be expressed as [50]

$$I_n(V_{sd}) = \frac{2e}{h}\left[\sum_{n_s}(E_F + \beta eV_{sd} - E_n)T_n - \sum_{n_d}(E_F + (1-\beta)eV_{sd} - E_n)T_n\right] \quad (2.44)$$

where E_n is the subband energy and T_n is the transmission probability. Assuming $T_n = 1$, the The differential conductance can be expressed as

$$G = \frac{dI}{dV_{sd}} = \frac{2e^2}{h}\left[\beta n_s + (1-\beta)n_d\right] \quad (2.45)$$

where n_s is the number of subbands such that $E_{n_s} < \mu_s < E_{n_s+1}$, and n_d is the number of subbands such that $E_{n_d} < \mu_s < E_{n_d+1}$. The differential conductance consists of the number of subbands from the source as well as the number of subbands from the drain that are occupied by electrons. From equation (2.45), it can be deduced that each time a subband crosses either μ_s or μ_d, the conductance increases by $0.5(2e^2/h)$.

Figure 2.3 shows that source-drain dc bias V_{sd} shifts the position of μ_s and μ_d relative to each other by $-eV_{sd}$. Figure 2.3 (a) shows when V_{sd} is less than the subband spacing of the 1D wire, the channel is conducting N modes in each direction and the differential conductance can be expressed in multiples of $G = \frac{2e^2}{h}N$. Figure 2.3 (b) shows when V_{sd} is increased, the transmission coefficient T(E) is N+1 for current at μ_s but is N at μ_d, the differential conductance can be expressed in multiples of $G = \frac{2e^2}{h}(N+1/2)$. Figure 2.3 (c) shows as the case where V_{sd} is increased further and eV_{sd} will reach the subband energy of the 1D wire. The transmission coefficient T(E) is N+2 at μ_s and N at μ_d, so the differential conductance can be expressed in multiples of $G = \frac{2e^2}{h}N$ where integer plateaus

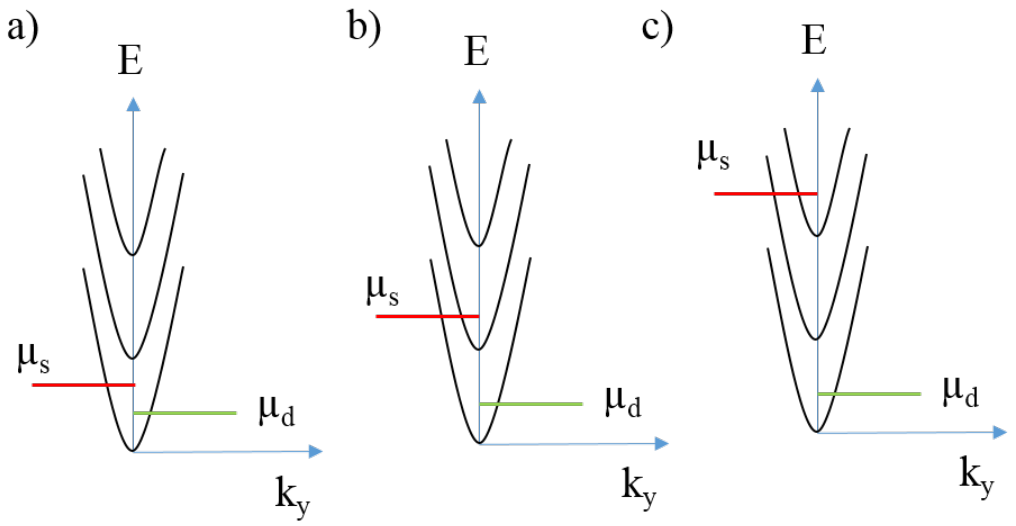

Figure 2.3: Schematic diagram of dispersion relation of three 1D subbands and chemical potentials of the source and the drain reservoirs when varying source-drain dc bias V_{sd}, is applied.

are observed.

2.7 Electron-Electron Interactions

The discussion in thesis so far of 1D transport of electrons has ignored electron-electron interactions in the 1D quantum wire. Quantisation of conductance in 1D wires in terms of $2e^2/h$ can be described in terms of a non-interacting model. However, the non-interacting model fails to account for anomalies in conductance such as the 0.7 structure which arise from many-body interactions.

The Hamiltonian of a many-body interacting system which includes the potential from the fixed nuclei in the crystal and the Coulomb repulsion between the electrons can be expressed as

$$H = -\sum_i \frac{\hbar^2}{2m_e}\nabla_i^2 - \sum_{i,I} \frac{Ze^2}{|r_i - R_I|} + \frac{1}{2}\sum_{i \neq j} \frac{e^2}{|r_i - r_j|} \tag{2.46}$$

where Z is the charge on the nuclei, m_e is the mass of the electron and R_I is the position of the I^{th} nuclei.

Approximations were developed to treat the effects of the nuclei in crystalline structures such as the Bloch theorem and the effective mass approximation and the effects of nuclei can be simplified as an external potentia acting on the electrons.

The electron-electron interaction term can be approximated as an potential from the charge of other electrons which is called the Hartree-Fock approximation. The total wavefunction of electrons can be written as a Slater determinant to satisfy Pauli exclusion principle and minimise the energy

$$\Psi_{r_1, r_2, \ldots, r_N} = \begin{vmatrix} \psi_1(r_1) & \psi_2(r_2) & \cdots & \psi_1(r_N) \\ \psi_2(r_1) & \psi_2(r_2) & \cdots & \psi_2(r_N) \\ \vdots & \vdots & \ddots & \vdots \\ \psi_N(r_1) & \psi_N(r_2) & \cdots & \psi_N(r_N) \end{vmatrix} \tag{2.47}$$

It can be shown that the Schrödinger equation of a single electron in a many-body state where r_m is the position of i^{th} electron [55–57],

$$\left[\frac{\hbar^2}{2m_e}\nabla_m^2 + \sum_{R_i}\frac{-Ze^2}{|r_m - R_i|}\right]\Psi_i(r_m)$$
$$+\left[\sum_{i,j} e^2 \int \frac{\Psi_j^*(r_n)\Psi_j(r_n)}{|r_m - r_n|}dr_n\right]\Psi_i(r_m) \tag{2.48}$$
$$-\left[\sum_{i,j} e^2 \int \frac{\Psi_j^*(r_n)\Psi_i(r_n)}{|r_m - r_n|}dr_n\right]\Psi_j(r_m) = E_i\Psi_i(r_m)$$

where m_e is the mass of the electron, Z is the charge on the nuclei, and R_i is the position of the I^{th} nuclei. The first term describes the Hartree Hamiltonian for non-interacting electrons and the second term describes the electron-electron interaction wave function. The last term of the equation (2.48) is the exchange interactions terms. The exchange term lowers the total energy and acts on electrons with the same spin. The exchange interaction aligns the electrons of the same spin due to Pauli exclusion principle and and so the Coulomb energy between the electrons is lowered.

2.8 Spin-Incoherent Transport

Luttinger liquid (LL) can be formed when electron-electron interactions are dominant and its behaviour varies from Fermi liquid. A major characteristic of Luttinger liquid is charge-spin where spin and charge modes have different group velocities to transport through the quantum wire. The conductance of the Luttinger liquid can change as a function of temperature and interactions [24]. When the energy of the spin excitation E_{spin} is exponentially suppressed relative to that of the charge excitation E_{charge} and the thermal energy k_BT lie between the two

energies such that $E_{spin} \ll k_B T \ll E_{charge}$, only the charge excitations are transmitted, giving rise to the spin-incoherent Luttinger liquid which is different from a normal Luttinger liquid.

In 2004, Matveev laid the theoretical foundations the spin-incoherent Luttinger liquid. He proposed that a Winger crystal with exponentially small exchange coupling J of neighbouring electrons is spontaneously formed in a quantum wire when the carrier density is extremely low, i.e., $n_e \ll 1/a_B$, where n_e is the carrier density and a_B is the Bohr radius [58, 59]. In this regime the electron spins are expected to give rise to a temperature-dependent resistance, which decreases exponentially with decreasing temperature and vanishes at $T = 0$. A spin-incoherent Luttinger liquid is characterised by the fact that if the temperature is higher than the characteristic spin scale and less than Fermi energy, spin becomes totally incoherent at a finite temperature while charge remains close to its ground state [60]. Such a system has distinction of having spin modes as well, therefore the conductance measurement shows plateau at e^2/h rather than the usual $2e^2/h$ [59, 61].

2.9 Spin polarisation in Quantum Wires

In 1D systems, Berggen *et al.* proposed that a large exchange interaction can occur when the Fermi energy passes through the subband threshold energies and drives a large subband splitting both in 1D wires [62]. The spontaneous spin polarisation which is dominated by exchange interactions was predicted to give rise to a spin-polarised at $0.5(2e^2/h)$ as only the spin down electrons transmit through the quantum wires. Thus, the spin polarisation of 1D subbands can

occur even in the absence of a large magnetic field in the lower subbands at low electron densities [62].

The calculations done by Berggen *et al.* at B = 0.01 T for an infinitely long quantum wire in the presence of in-plane magnetic field. At low densities, the 1D wire can be fully spin polarised and the first conductance plateau is expected at $0.5(2e^2/h)$. When spin polarisation occurs as the density is decreased by sweeping the gates, the effective transmission barrier becomes different for the two spin directions [63]. When spin polarisation occurs at low densities, the conductance should be equal to or larger than $0.5(2e^2/h)$ but the exact value may be device dependent. The spin splitting is caused by the exchange potential and not by the Zeeman splitting. Berggen *et al.* have done further calculations using a finite-length 1D quantum wire instead and also the potential was modelled as a saddle-point and it confirmed that spin polarisation occurs as the electron density is lowered and thus the effective barrier height is different for spin up and spin electrons [63, 64].

2.10 Summary

This chapter has given an introduction to different aspects of theory work relevant to the work presented in the thesis. Additional theory specific to the work presented in individual chapters is presented at the beginning of each chapter.

Chapter 3

Measurement Techniques and Apparatus

3.1 Introduction

Transport measurements in quasi-1D quantum wires are usually performed by measuring the conductance by applying a differential voltage across the 1D wire. To create a quasi-1D constriction, a negative voltage is applied to the arms of the split-gates. The width of the 1D wire can be changed by tuning the negative voltage applied to the split-gates. Typical quasi-1D wires usually have subband spacing of around 1-5 meV therefore for the quantised plateaus to be observable measurement parameters such as noise, temperature and excitation voltage should be comparable or less than the subband spacing of the 1D wire.

The thermal energy, kT, at room temperature is around 25.7 meV and thus thermal broadening of the Fermi level will destroy any quantisation of plateaus and any phenomena due to electron-electron interactions which have energies smaller than the subband spacing. Thus, samples should be cooled down to milli-kelvin temperatures in order to observe the quantum effects. In this thesis, apart from differential conductance measurements, other measurement methods have been performed to characterise 1D wires such as temperature and magnetic

field dependence effects and subband spectroscopy using a dc source-drain bias method. The devices were initially tested at 2.4 K before loading in a dilution refrigerator for further detailed measurements.

3.2 Low-temperature Measurements

3.2.1 Cryogenic Liquids

Devices can be tested at lower temperatures by immersing them in cryogenic liquid like liquid nitrogen (77 K) or liquid helium (4.2 K) using a home-made probe. At liquid nitrogen temperature (77 K), the resistance of the Ohmic contacts can be measured to check the reliability of the contacts where the two-dimensional electron gas has been formed. Lower temperatures can be accessed by either immersing the device in liquid helium (4.2 K) or using a cryogen-free (2.4 K) assessment cryostat to test the samples (see figure 3.1 (b)). At lower temperatures, the split-gates devices can be tested by sweeping the split-gates using negative voltages to see if a 1D wire has been created. The quantised plateaus are usually not visible for split-gates devices as the temperature is high due to thermal broadening. Additional gates patterned on the device to control the density of the wire like a mid-line gate, top gate or a back gate can also be tested. At this assessment stage, the devices are also tested for any possible leakage through the gates and contact resistance of the Ohmics with the 2DEG. If the device shows basic appreciable characteristics and most gates are working, the sample is ready for detailed measurements at dilution temperatures.

3.2.2 ^{3}He/^{4}He Cryostat

Temperatures sub 4.2 K can be achieved by using a multi-stage pulse tube refrigerator and helium gas. Oxford Instruments Teslatron cryostat works by having a pulse tube that cools down the system and transfers heat outside the system. Helium gas is usually compressed in an external compressor to avoid mechanical noise and the gas is sent back into the pulse tube. The pulse tube can get the cold plates in the cryostat to temperatures less than 4.2 K and in addition the cryostat has a separate ^{4}He cooling circuit that brings down the base temperature to 1.5 K. The boiling point of liquid helium varies depending on the pressure and at 1 atm liquid helium-4 has a boiling point of 4.2 K and reducing the vapour pressure will lower the liquid helium boiling point. A rotary pump can be used to achieve this by pumping the helium gas above the helium liquid and thus cooling the system down to 1.5 K. By using He-3 gas which has a lower boiling point instead of He-4, a lower temperature down to 300 mK can be achieved using Heliox He-3 insert probe. The Heliox probe works by continuous pumping of the condensed ^{3}He vapour thus reducing the vapour pressure and lowering the temperature to reach a base temperature of 300 mK. The advantages of a Helium-3 system is that it is easy to use and has a quicker sample turn-around time than a dilution refrigerator. The Teslatron cryostat contains a superconducting magnet, capable of reaching a magnetic field of 8 T. The temperature of the system can be set to any temperature using heaters placed near the samples at the cold finger.

3.2.3 The Dilution Refrigerator

The dilution refrigerator is an advanced, sophisticated piece of engineering and can have a base temperature of 10 mK. The dilution refrigerator works by using a mixture of ^{3}He and ^{4}He and when it is below a critical temperature (870 mK), it separates into two phases; the concentrated phase which is a rich ^{3}He phase and a mixed ^{3}He/^{4}He phase. The dilution refrigerator operates by ^{3}He diffusing from the pure phase into the mixed phase in a mixing chamber and this has a cooling effect as the dilution is an endothermic process. He-3 is then extracted as a gas from the chamber and then re-condensed and re-injected into the pure phase in a closed cycle to provide continuous cooling in the fridge. The results presented in this thesis were measured in a cryogen-free dilution refrigerator with a base temperature below 10 mK with a superconducting magnet capable of a maximum field of 14 T (see figure 3.1 (a)). The sample sits in vacuum and it is not immersed in ^{3}He/^{4}He mixture and the thermal contact with the mixing chamber is made through the wiring in the system. The base temperature was measured to be 10 mK and the corresponding electron temperature was estimated to be 70 mK.

3.2.3.1 The Sample Holder

The sample holder consists of an LCC (leadless ceramic chip) open top socket holder which provides easy loading of the device and high spring force of pins assure excellent side contact with the LCC. The pins of the LCC socket are then soldered to a custom PCB board and connected to a nano-cinch connector. All connectors and the gold plating of the PCB are non-magnetic (nickel-free) to prevent magnetic hysteresis when magnetic field is applied. The sample holder

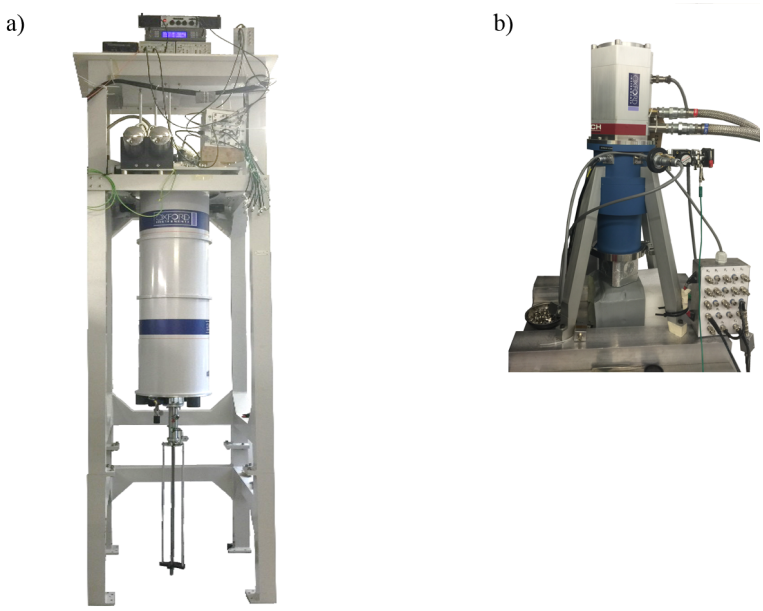

Figure 3.1: a) A photograph of the cryogen-free dilution refrigerator, Triton-400 which has 52 dc lines and 8 RF lines and a base temperature of 8 mK. b) A photograph of the cryogen-free cryostat, Oxford He-4 system which has 24 dc lines and 4 RF lines and a base temperature of 2.4 K.

design was compact enough to fit into the sample space inside the puck. The sample holder is extremely versatile and could be used to measure samples in both in-plane and perpendicular magnetic field orientations to performing RF as well as dc measurements. Also, a red LED is placed opposite to the sample for illumination of the device. The sample holder was made from oxygen-free copper which is less likely to oxidise and degas than normal copper. Figure 3.2 (b) shows a 3D prototype of the sample holder design that fits inside the puck.

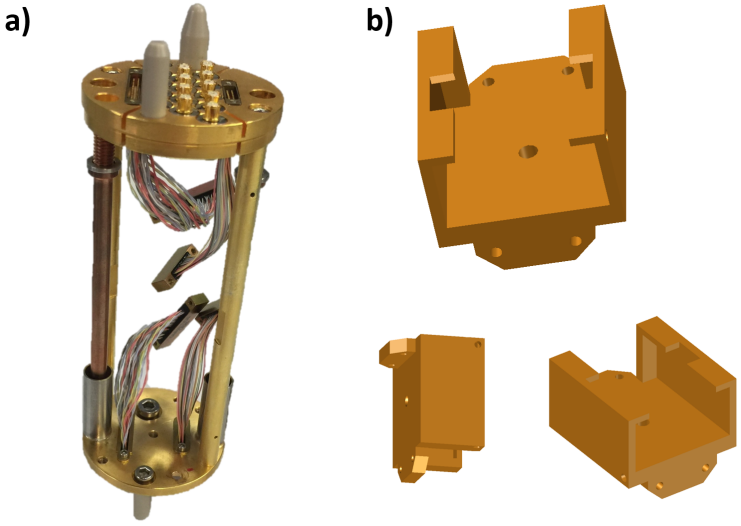

Figure 3.2: An image showing the design of the puck that fits in the cryogen-free dilution refrigerator, Triton-400 which has 52 dc lines and RF lines. b) the schematic diagram of the sample holder in both in-plane and perpendicular magnetic field orientations.

3.2.4 Electrical Measurements

1D devices are characterised at low temperatures using electrical measurements. To observe quantum effects, it is essential to keep the voltage and currents quite low, typically I = 10 nA, and V = 10 μV so the energy scale of 1D wire is not exceeded and a small excitation is important to avoid any significant electron heating. The electrical noise can be eliminated greatly by using phase-sensitive detection of a sinusoidal excitation. A lock-in amplifier consists of a detector coupled to a narrow-bandwidth low pass filter that can extract a signal with a known carrier waveform from a very noisy signal. As a result, noise elsewhere in the power spectrum can be largely eliminated.

3.2.4.1 Two-terminal measurements

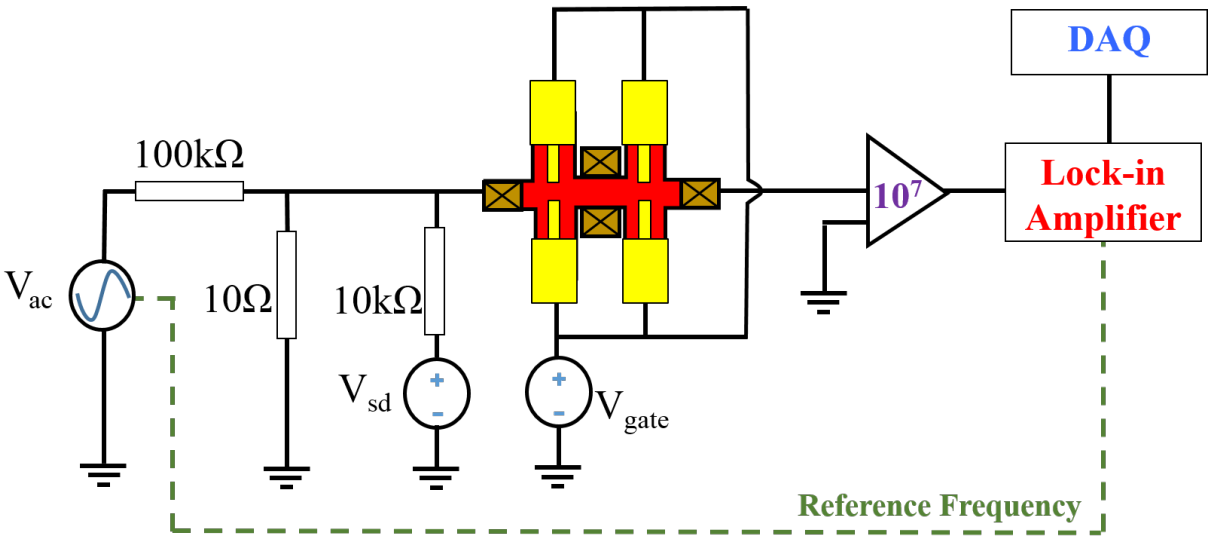

Figure 3.3: Electrical circuit of a typical two-terminal differential conductance measurement where the current is measured as a function of gate voltage. The source-drain bias, V_{sd}, is usually set to zero but a finite bias may be applied in a source-drain bias measurement.

The data presented in the thesis is obtained using a two-terminal measurement circuit as shown in figure 3.3. A potential divider circuit is used to set the voltage across the sample to a constant value of 10 μV. After the current passes through the sample ($\sim$ 10 nA), it is amplified using a current to voltage pre-amplifier. Then, the output voltage from the current pre-amplifier is fed to a lock-in amplifier, which detects the signal at a given reference frequency of 77 Hz. This signal is passed to a measurement computer over a GPIB interface. Since the bias voltage is constant, it is proportional to the conductance of the sample as well as a series resistance contribution. The circuit can be calibrated by using a resistor of a known value instead of the sample usually a 10 kΩ resistor. The signal measured by the lock-in amplifier is then scaled so the signal corresponds to the

conductance in units of μS. Dc-bias measurements can be performed by adding a dc signal to the excitation voltage at the potential divider using additional circuitry. A DAC is used to provide a split-gates voltage to control the carrier density inside the quantum wire. RC filters, which normally consist of two 1 MΩ resistors and one 0.1 μF capacitor are connected between the DAC and the sample to cut off high-frequency noise.

3.2.4.2 Series Resistance

When using the two-terminal measurement technique, the measured signal includes the resistance of the connecting wires, the 2DEG, resistors in filters, and Ohmic contacts. In order to determine the actual 1D conductance, it is important to remove the contribution of all additional resistances in series with the 1D wire. The Ohmic contacts are considered to be the highest contributors to series resistance. The conductance of the 1D wire in units of $2e^2/h$ is given by

$$G = \frac{1}{(\frac{1}{G_m} - \frac{1}{R_s}) \times 77.27 \times 10^{-6}} \tag{3.1}$$

where G_m is the measured conductance, and R_s is the series resistance and the value of R_s is chosen at definition of 1D wire. The subtraction of series resistance will make the quantised plateaus align to their known quantised values known as the quantum resistance. An approximation of the value of R_s is given by the resistance of the sample when no voltage applied to the gates. Alternatively, a value of R_s can be chosen which best aligns the conductance plateaus to their known quantised values

3.2.4.3 Four-Terminal Measurements

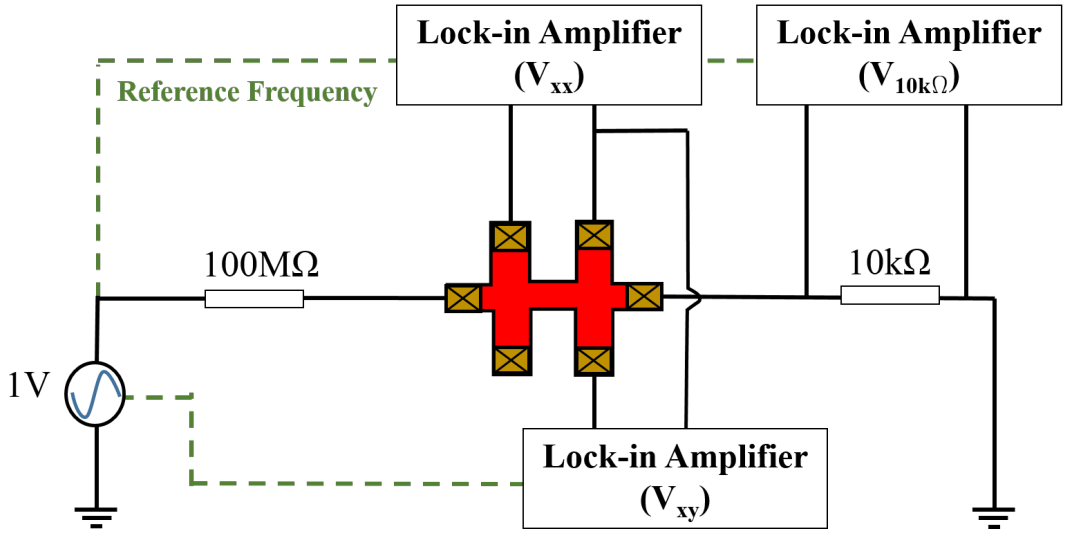

Figure 3.4: Four-terminal measurement measurement circuit where transverse (V_{xy}) and longitudinal (V_{xx}) voltages are measured which show the Quantum Hall effect and Shubnikov-de Haas oscillations. Optionally, the current can monitored by measuring the voltage across a 10 kΩ resistor.

A four-terminal measurement removes the need to correct the series resistance as the current is passed through the 1D quantum wire and then using separate probes to measure the voltage dropped across the wire where no current flows. The four terminal measurement set up can be used for magnetotransport measurements such as Quantum Hall and Shubnikov-de-Haas oscillations. The Hall bar is connected in series with a very large resistance 100 MΩ where the constant-current approximation holds true as the resistance of the Hall bar remains low in comparison to the resistor used and therefore current remains constant around 10 nA.

Figure 3.4 shows a four-terminal measurement circuit and the resistance across the sample is measured directly. The Hall (R_{xy}) and longitudinal (R_{xx}) resistances

of a 2DEG are measured using separate lock-in amplifiers which show the Quantum Hall effect and Shubnikov-de Haas oscillations. The carrier density (n_{2D}) of the 2DEG in the GaAs heterostructure can be extracted from the slope of the Hall resistance using

$$n_{2D} = j\frac{2eB}{h} \tag{3.2}$$

where e is the charge on an electron, B is the magnetic field and j is the filling factor. Optionally, the voltage across a 10 kΩ output resistor can be monitored to check that the current is indeed constant and this method is not routinely used to measure 1D systems as the sample resistance increases towards pinch off so a large voltage is dropped across the device.

3.2.4.4 Noise Reduction Techniques in electronic systems

Noise reduction and elimination is extremely vital for sensitive low-temperature measurements. The lock-in technique reduces the noise in the measured signal greatly by detecting the signal at a specific frequency and eliminates the rest of the signal from the spectrum. The signal frequency of the source-drain voltage is chosen to be far from the mains frequency which is 50 Hz and its higher harmonics. The output signal should be checked using a spectrum analyser before measurements are carried out to check for noise in the circuit. 50 Hz and RF noise are considered to be the main source of noise in the electrical measurement system. The laboratory was designed in such a way that the entire laboratory was contained in a Faraday cage. RF tests were done in the lab and the surrounding

areas and it was found to have a minimum presence of RF frequencies and comparatively lesser 50 Hz presence than the open area on Gordon Street. RF noise leads to heating up of electrons and thus increases effective electron temperature. 50 Hz (and higher harmonics) noise arises from ground loops and electronic equipments being connected to the mains. Ground loops can often lead to significant noise levels and to ensure that these did not occur all electronic equipment and the cryostat were floated with the exception of the oscillator which was earthed to the mains earth via a filtered supply. Ground loops can be eliminated by ensuring that there is a common ground for all the measurement instruments and placing an isolating transformer between the electronic rack and the power supply. Also, a low resistance clean earth rod needs to be installed and the earthing rod needs to be placed deep in the ground and away from other earthing rods. All such requirements were taken care of, and the laboratory had a dedicated clean earth bar. Special care was taken by having independent power lines for non-essential items such as pumps to save devices from blowing up. In addition, low-pass RC filters should be connected between the gates and the voltage sources to remove any RF noise.

3.2.4.5 Measurement Apparatus Data Acquisition and Analysis

Several pieces of electronic equipment were used to obtain the data presented in the thesis. Sinusoidal excitation at 77 Hz was generated using a Krohn-Heit 4402b ultra-pure sine wave analogue signal generator. Digital lock-in amplifiers (Signal Recovery model 7265) were used in the course of this work. Different types of pre-amplifiers were used, depending on the measurement set-up. For current-to-voltage amplifiers, a Stanford Research systems low-noise current pre-amplifier

model SR570 was used. For voltage measurements, a Stanford Research systems low-noise voltage model SR560 differential-voltage pre-amplifier was used. To provide dc voltages for the gates and a source-drain bias, a national instruments 9269 four-channel 16-bit resolution digital-to-analogue converter was used with an output voltage range of up to ± 10 V. For dc voltages beyond 10 V, a Keithley Model 2636B system SourceMeter was used with an output voltage range of up to ± 200 V. Temperature measurement and control was done by a Lake Shore 370 AC resistance bridge. The magnet in the cryostat was controlled by an Oxford Instruments mercury ips superconducting magnet power supply.

3.2.4.6 Data Acquisition and Plotting

All measurement instruments were connected to dedicated measurement computer and controlled through a GPIB interface using National Instruments LabVIEW CryoMeas which is a data-acquisition programme developed by Prof Chris Ford from Cavendish Laboratory. Greyscale and graphical figures were generated using software built using MATLAB called "My plotter" which was developed and written by me. The multi-tasking software has capabilities of removing the series resistance, filtering noise from data, producing differential plots and saving graphs in several formats.

3.3 Summary

In this chapter, low-temperature measurement techniques performed in this thesis are discussed. The measurements presented used a variety of cryogenic systems where the devices were initially tested at 2.4 K and devices which were deemed

suitable were further tested using a dilution refrigerator.

Chapter 4

Fabrication

4.1 Introduction

A quasi-1D quantum wire can be realised using a split-gate technique formed on the surface of a GaAs/$Al_xGa_{1-x}As$ heterostructure. A modulation-doped HEMT which has a 2DEG at the interface of GaAs/$Al_xGa_{1-x}As$ is the starting point for the fabrication of split-gates devices. A mesa is etched into the wafer to electrically isolate a region of the 2DEG, and then Ohmic contacts are deposited to form electrical contact to the 2DEG. Metallic gates are then patterned onto the surface of the wafer by photo-lithography or electron-beam lithography (EBL), and metallised in an evaporator. Additional layer of an insulating dielectric may be deposited on the split-gates to create a top gate that lies directly above the split-gates. This section describes the process flow of fabricating a device, starting from an unprocessed GaAs wafer to a final packaged device. The basic process includes cleaning, etching the mesa, patterning and metallising the Ohmic contacts and optical gates, performing EBL to create split-gates and additional gates as required.

4.2 Cleaving

The wafers used are GaAs/$Al_xGa_{1-x}As$ wafers with growth orientation <100>. The maximum mobility of the device is achieved by aligning the chip parallel to the major flat. Subsequently, the mesa should be aligned also parallel to the major flat of the wafer. When cleaving the sample, it is important to indicate the major flat either by scribing a rectangular chip in which the longer edge is parallel to the major flat or scribe a line on the backside of the chip indicating the crystal orientation.

4.3 Scribing

III-V materials including GaAs are delicate and are cleaved along the crystal plane easily. Scribing is done using a stepped cleaving block where the cleaved line on the chip is aligned to the step of the cleaving block and a light pressure is applied to one side of the chip while holding the other side of the chip using either wafer tweezers or glass slide wrapped in a clean wipe to avoid scratching of the surface.

4.4 Cleaning

After the GaAs wafer is scribed and cleaved into the required size for processing, it is cleaned before starting the fabrication process. The main purpose of cleaning the GaAs wafers is to remove any contaminates such as organic compounds and metal ions off the surface. Organic solvents are used to remove any organic contamination off the surface. Sonification of solvents using ultrasonic bath along-

side heating them enhances the cleaning efficiency. The cleaning process follows a strict sequence of treatments with different organic solvents:

1. 10 minutes in methyl-ethyl-ketone
2. 10 minutes in acetone
3. 10 minutes in methanol
4. 10 minutes in ethanol
5. 10 minutes in IPA

For removal of ion containments, samples are immersed in pure de-ionised (DI) water bath (18 MΩ) for 10 minutes.

4.5 Optical Lithography

The term photolithography can be divided into two parts; firstly is photo which means the application of light and lithography to deposit patterned metal of metal. Lithography carried out by applying a source of light is called photolithography. Photolithography was done using a Karl Suss MB-3 photolithography machine with chrome plated glass masks. Figure 4.1 shows the schematic design of the optical mask used to make mesa, Ohmics and gates. The aligner works by having a photosensitive resist layer on the sample that is exposed to ultraviolet (UV) light through a desired pattern created by a mask for metal lift-off or etching. A photolithography recipe has been developed in the present work and optimised to be reliable which gives a large undercut profile to make lift-off easier. Without an edge bead removal step, the resolution of the features is ~ 2.5

μm and with edge bead removal, the resolution was improved to ~ 1 μm. On the other hand, EBL is used to pattern sub-micron features in split-gates devices.

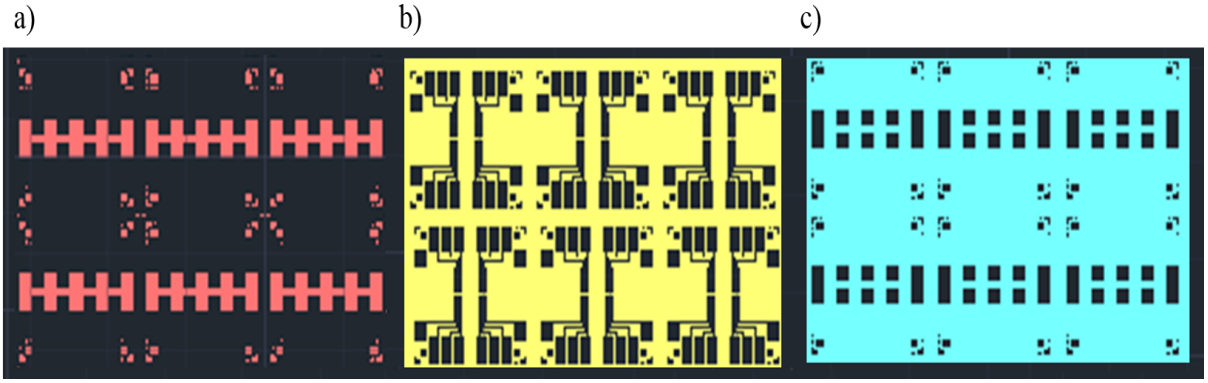

Figure 4.1: A schematic diagram of optical mask showing the a) mesa b) gates c) Ohmics.

4.6 Hall Bar

The aim is to define the mesa using optical lithography and then etch through the sample beyond the 2DEG to electrically isolate the device and leave a raised mesa. The sample is prebaked at 125°C for 60 seconds to remove any water or solvent residual and to promote adhesion of the photoresist. The chip is coated with Shipley S1805 negative resist which gives nominal thickness of 500 nm. The chip is spun at 500 rpm for 5 seconds and then 7000 rpm for 30 seconds and baked for 60 seconds at 115°C. The smaller the chip size, the faster the spinning speed of the photoresist has to be to reduce edge-bead. Mask aligner is used to align the mesa parallel to the crystal orientation and pass UV through the patterned mask and on the chip. The mesa is developed in MF-319 developer for 45 seconds and then rinsed in DI water bath to stop further developing. Figure 4.2 shows a

fabricated Hall bar with mesa etched and Ohmic contacts deposited.

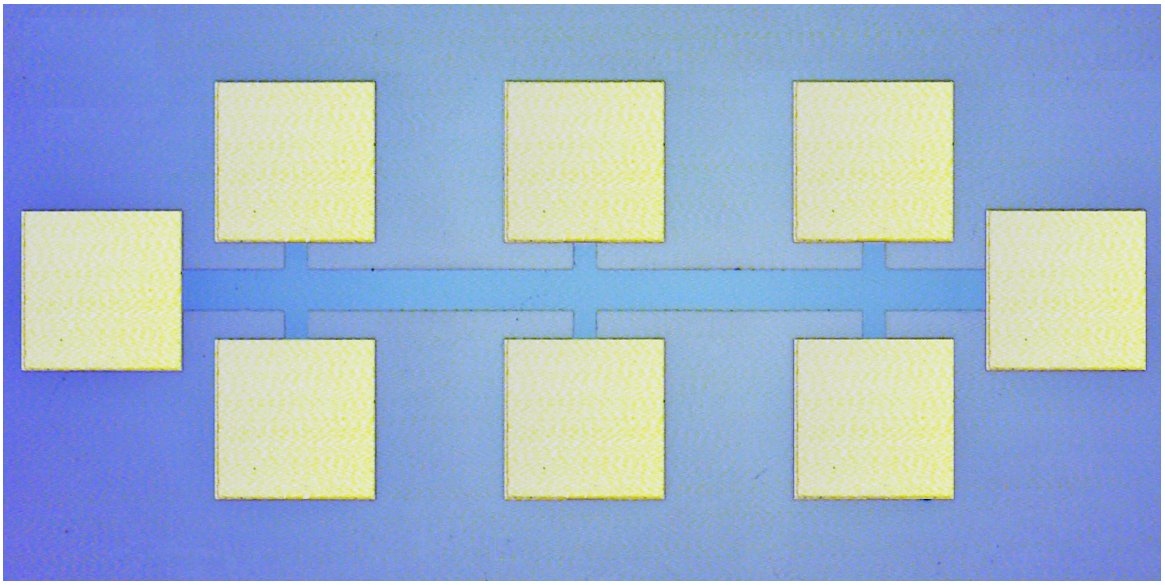

Figure 4.2: A typical Hall bar with source and drain contacts and side Ohmics. The typical dimensions of the Hall bar is 1800 μm in length and 80 μm in width.

4.7 Etching

Etching is required for the formation of mesa structure and for electrical isolation from the adjacent devices on the same wafer. The mechanism of the wet etching is the oxidation of the surface to form As oxide and Ga oxide followed by the dissolution of these oxides by chemical attack with acid. Hydrogen peroxide (H_2O_2) is usually used as an oxidizing agent to create the surface oxides. The main aspect of choosing the etch solution is the etch profile, the etch rate and the critical dimension. $H_2O : H_2O_2 : H_2SO_4$ etchant is used in etching the mesa and the mixture is 120:8:1 which means one part of sulfuric acid, eight parts of hydrogen peroxide and forty parts of water which altogether gives an etch rate

of 10 nm/s. This is a popular etchant used for etching GaAs/$Al_xGa_{1-x}As$ wafers [65–67]. The depth of mesa is then measured using a Dektak surface profiler to check whether the height of the etched mesa has passed the 2DEG.

4.8 Lift-off

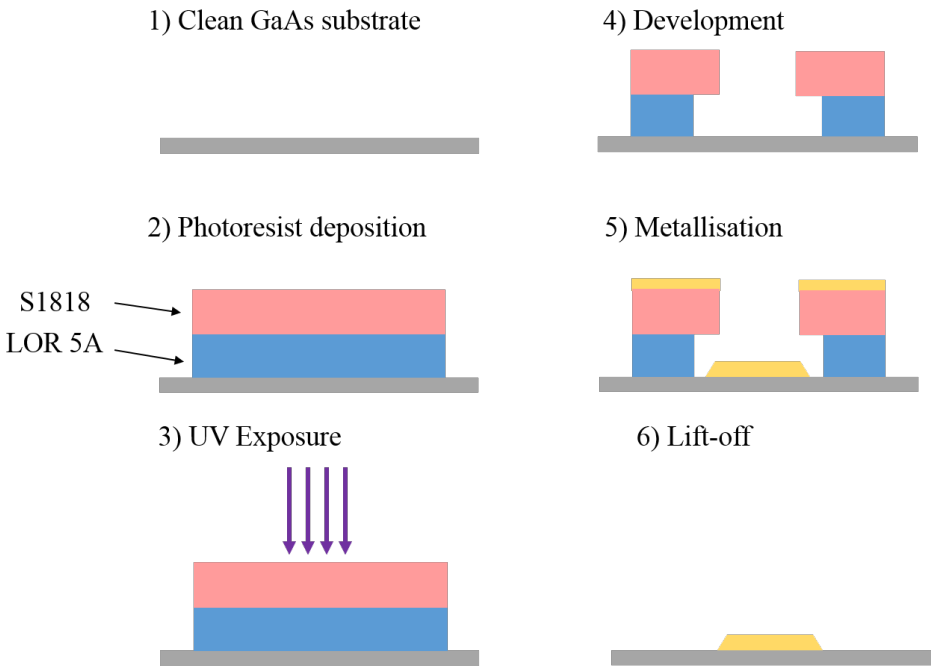

Figure 4.3: A schematic diagram to show the steps of a lift-off process for metal deposition on GaAs substrate using a bi-layer resist. The bi-layer resist method creates an undercut profile and then the resist is stripped off in a solvent, leaving the deposited metal on the semiconductor surface.

The photolithography recipe used for lift-off consists of a bi-layer of photoresists MicroChem LOR-3A and Shipley 1818. The LOR-3A is spun at 500 rpm for 5 seconds and then 7000 rpm for 45 seconds and baked for 10 minutes at 170°C followed by spinning S1818 at 500 rpm for 5 seconds and then 7000 rpm for 45

seconds and baked for 60 seconds at 115°C. The sample is developed in MF-319 developer for 60 seconds. This process produces relatively high undercut rates which makes it better suited for thick film and large feature deposition. The Remover 1165 from Shipley is used as the resit stripper and the lift-off. Acetone is not allowed to be used with LOR resist as LOR reacts with the acetone and expand producing a cross-linked material with the appearance of latex. Figure 4.3 shows a schematic diagram of the process of lift-off to deposit metal on GaAs substrate.

4.9 Ohmic Contacts

4.9.1 Introduction

Ohmic contacts are an important element in a device as it is required to get information out of a 2DEG system which is investigated by electrical measurements. Nearly all semiconductor/metal interfaces have barriers to carriers. The important part in fabricating an Ohmic contact is to design these barriers to be low for electrons tp cross the barriers by thermionic or field emission. The barrier occurs because of the band bending in the valance and conduction band as a result of electronic states at the semiconductor and metal interface.

Au/Ge/Ni alloyed Ohmic contacts are popular choice to make an Ohmic contact to 2DEG in the GaAs/$Al_xGa_{1-x}As$ heterostructures. Au/Ge/Ni alloyed contacts have been originally used as a contact for n-doped GaAs and were later used in GaAs/$Al_xGa_{1-x}As$ heterostructures. There are many recipes for Ohmic contact to GaAs and there is no mechanism understood well enough to produce

systematic Ohmic contacts. Every fabrication lab needs to optimise the fabrication methods to produce stable and robust Ohmics contacts. In the present work, Ohmic fabrication methods have been optimised in the LCN cleanroom and was later passed on to other colleagues. In this chapter, electrical and structural properties of alloyed Au/Ge/Ni contacts to the 2DEG will be discussed.

4.9.2 Physics of Ohmic Contacts

Metal-semiconductor contacts fall into two categories of interest in the physics of device fabrication, the Ohmic contact which is the subject of this section and rectifying (Schottky) contacts which are used for gate fabrication.

When a metal is deposited as a contact with a semiconductor such as GaAs, the conduction and valence band bend to make the Fermi levels in the semiconductor and metal align as shown in figure 4.4. Electrons move from the material with the lower work function to the material with higher work function till their Fermi levels align. The material with the lower work function will be positively charged (semiconductor) comparatively to the material of higher work function which becomes negatively charged (metal). The band bending causes a potential across with the contact between the metal and semiconductor. The aim with Ohmics fabrication is to reduce band bending and work function differences so electrons can move freely across the junction. Surface states occur in the forbidden gap between valence and conduction bands due to the abrupt change at the interface of the semiconductor crystal and the deposited metal. These highly dense surface states sets the barrier height for current to flow across the interface.

The potential barrier depends on the work function of the metal, ϕ_m, the work

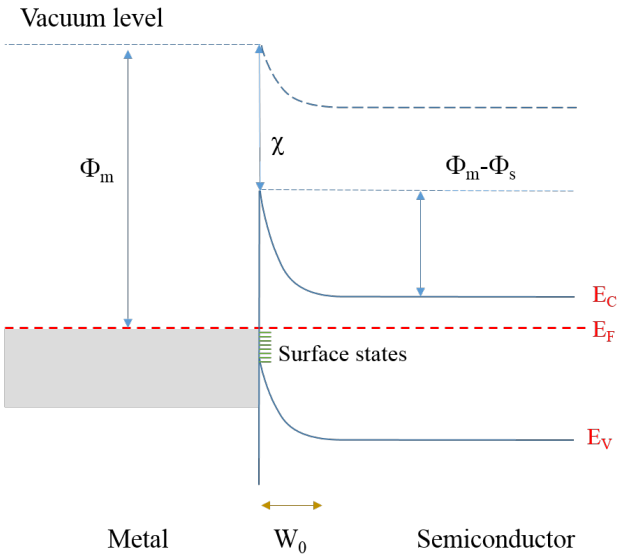

Figure 4.4: Metal-semiconductor junction showing barrier height as difference between the work function of metal ϕ_m and electron affinity χ. The diagram shows the surface states tend to pin the Fermi level.

function of the semiconductor, ϕ_s, and electron affinity, χ. The work function, ϕ, of the material is the difference between the Fermi energy E_f and vacuum level; the energy needed to remove an electron to infinity. The potential barrier for electrons to flow from metal is $\phi_m - \chi$. However, the potential barrier for electrons to flow from semiconductor to metal is $\phi_m - \phi_s$. The surface state density at the metal-semiconductor interface sets the bending of the conductance band and barrier height for electrons to flow across. This is a function of the semiconductor and independent of the metal.

Electrons may cross the potential barrier by having enough thermal energy to pass over the barrier which is called thermionic emission or if the barrier is narrow enough electrons can pass over by quantum mechanical tunnelling [68, 69]. A combination of both is named as thermionic-field emission [70].

In thermionic emission, a fraction of the electrons have sufficient thermal energy to cross the barrier and the current due to thermionic barrier emission is given by [71]

$$\begin{aligned} J &= A^{**}T^2 exp(\frac{-q\phi_b}{kT})[exp(\frac{qV}{kT}) - 1] \\ &= J_s[exp(\frac{qV}{nKT}) - 1] \end{aligned} \tag{4.1}$$

where A^{**} is the effective Richardson constant, T is the absolute Temperature, q is the electron charge, ϕ_b is the barrier height, k is Boltzmann constant, V is the voltage across the barrier and n is the ideality factor which represents the departure from an ideal Schottky barrier. From equation 4.1, it can be see that low current arises from low voltages.

The other mechanism for current to flow across the barrier is field emission which allows quantum tunnelling through the potential barrier. As the doping in the semiconductor increases, the width of the barrier decreases and tunnelling can occur [72, 73]. The equation of the current from the field emission is given by [71]

$$J = exp(\frac{-q\phi_b}{E_{00}}) \tag{4.2}$$

where E_{00} is a constant that is material dependant and can be expressed as

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N}{\epsilon m^*}} \tag{4.3}$$

where is $\hbar$ is plank constant divided by 2π, ϵ is the dielectric constant, N is the doping factor, m^* is the effective mass. From equation 4.3, the current increases as the square root of the doping concentration.

In reality, thermionic, field emission and thermionic-field emission exist for current to pass through the barrier and the origin of the contact resistance. From equation 4.1 and 4.3, making an Ohmic contact can be achieved by either lowering the barrier height or increasing the doping concentration. To make an Ohmic contact, the surface of the semiconductor should be doped to ensure that dominant conduction mechanism is the field emission tunnelling. The presence of a sufficient highly doped material between the metal and lower doped semiconductor is a necessary condition to achieve a good Ohmic contact [74]. Metals that can highly dope the surface layer of the semiconductor upon alloying and germanium can be one of these metals [75].

4.9.3 Metallurgy of AuGe/Ni Ohmics

Nickel, Germanium-gold and gold are the dominant and most common n-type contacts to GaAs [72]. The recipe for alloyed AuGe/Ni/Au to n-GaAs was introduced by Braslau in 1966 [76]. The metallurgy of a Au/Ge/Ni contact can be described in several steps. Firstly, Ni in the metal contact reacts with the native oxide on the GaAs surface. The native oxide on GaAs is difficult to characterise and can change in an unreproducible way which can cause inconsistency in the fabrication process. Surface treatment of GaAs before metal deposition is vital and will be explored further in section 4.9.11. Ni is intended to be used as a wetting agent and prevent AuGe from balling up during annealing process [77, 78].

Ni is an important component as it reacts with different types of oxide on GaAs surface. AuGe contacts without Ni have poor contact resistance, morphology and large variations in contact resistance.

Au and Ge are used in their eutectic composition 88% Au and 12% Ge by weight and this composition gives the lowest melting point of 361°C while Au has its melting point of 1064°C and Ge has a melting point of 938°C. It is vital that the entire AuGe should be evaporated to dryness to ensure that the correct stoichiometry has been deposited on the GaAs wafer chip, otherwise, the Au/Ge ratio may not be correct and result in poor reproducibility.

Applying a gold coating on top of AuGe/Ni is important as the annealed NiAuGe has poor sheet resistance and adding a subsequent gold layer is good to reduce the sheet resistance. Wire bonding or probing of NiAuGe without a gold coat is difficult as it is sensitive to the exact place the bond or the probe is placed. A layer of Au on top of AuGe/Ni is important as it improves surface morphology and enhances the effect of making more uniform Ohmics.

4.9.4 Annealing of NiAuGe Contacts

The annealing process of AuGe is very complex and not fully understood. A qualitative description below is generally believed to occur during annealing. Typically thermal annealing of the contacts occurs at around 450°C for 20 seconds to several minutes. Usually, shorter times require higher temperatures than longer times. The heating of the metallisation is accomplished by using a rapid thermal annealer (RTA), although furnaces, ovens and strip heaters can also be used. An RTA machine should have an inert chamber usually made from quartz, a heater

and a supply of inert gas like nitrogen or forming gas. The chamber of the RTA machine should be purged with a high purity inert gas to remove oxygen as Ni and Ge can oxidise and increase the contact resistance. Another important factor in the annealing process is the sample placement.

As the temperature is increased, Ni diffuses into GaAs and reacts to form intermediate Ni-GaAs complexes decomposing the GaAs and helping inter-diffusion of AuGe into GaAs. The intermediate complexes disturbs the crystal lattice for diffusion of other atoms and further reactions. Without Ni, the contact will require more thermal energy for Au and Ge to get started. Ni-GaAs complexes disturb the crystal lattice and the way is prepared for Ga to diffuse in the GaAs [72, 79]. Ni-Ge-GaAs complexes help the substitutional-interstitial diffusion into the Ga vacancies to occur at lower temperatures between 100°C and 450°C [2]. The diffusion of Ga into GaAs leads to high doping levels that makes tunnelling through the contacts possible. At temperatures higher than 250°C, the Au-Ga reaction is kinetically favoured and it will continue until the supply of Au is exhausted. Reactions between the metal and GaAs continue to form intermediate compounds like NiAs and NiGe. Excess As transport to the surface where it either resides or vaporises. Voids formed by loss of As are filled with different compounds like AuGe and NiGe. The annealed Ohmic contact should show a textured surface as some areas will be lower in height where the contact has spiked and As has been consumed.

Kuan *et al.* performed a transmission electron microscope (TEM) and X-ray diffraction (XRD) analysis on NiAuGe contacts [2]. Figure 4.5 shows the chemical composition of contact at a later stage of annealing via XRD. There are two different areas which are present; firstly a Au rich phase having Ni, Ga

and As phase called as Ni_2GeAs. The low contact resistance is credited to the distribution of a Ni_2GeAs/GaAs regions at the interface layer of GaAs where heavily doped regions a created due to the diffusion of Ge. The higher contact resistance can be related to the dominance of the Au/GaAs areas at the interface of the contact.

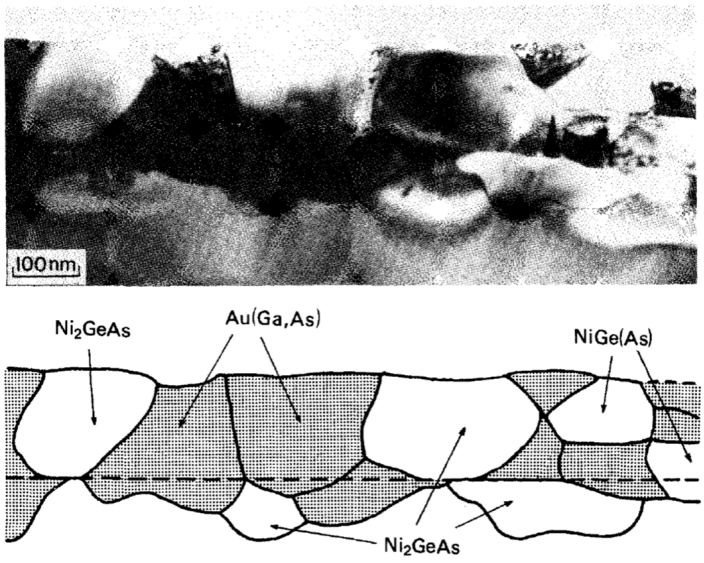

Figure 4.5: A cross-section TEM image of an NiAuGe annealed contact. The distribution phases and chemical composition of the contacts are shown in the sketch below the image [2].

The resistance of the NiAuGe contact depends on the annealing conditions of the contact. Annealing of NiAuGe usually happens at temperatures higher than the AuGe eutectic melting temperature which is 360°C. The resistance of a NiAuGe contact is usually high for short annealing times, then the contact resistance decreases for moderate annealing times in order of minutes before starting to rise again for annealing times beyond the optimum duration. Thus, a critical control of the annealing process is required to obtain reliable and reproducible

Ohmic contacts.

An optimisation process is required to determine the optimum temperature and duration of the GaAs. There is a significant variation in time and temperatures used by various groups. This discrepancy can be caused by the difficulty to determine the temperature of the wafer accurately. The temperature is monitored usually at the oven or the sample holder. The temperature recorded in the annealer differs from that of the wafer. The optimum temperature will depend on the chamber size, heating configuration and gas flow. The optimum time and temperature will depend on the cooling and the heating condition of the chamber. For these reasons, an optimisation process of the annealing recipe should be done by performing a series of experiments in which parameters of the annealing temperatures, times and contact composition are varied. Then for each variation, the contact resistance is measured.

4.9.5 Recipe of NiAuGe Contacts

Various contact recipes have been used by different research groups to produce a reliable, low-resistance and reproducible Ohmic contacts to 2DEG in GaAs/$Al_xGa_{1-x}As$ heterostructures [80–87]. The metal contact areas to be annealed are defined by optical lithography. The samples are placed for 60 seconds in an O_2 plasma asher followed by an oxide removal step where the sample is dipped in HCl for 10 seconds followed by dip in a DI water bath. The samples are loaded quickly (less than a minute) in the evaporator to avoid oxide regrowth on the surface. AuGe followed by Ni and then Au are deposited using thermal deposition in high vacuum. Then the sample is left in 1136 solution to remove

the photoresist. Annealing of samples was done using a rapid thermal annealer (RTA) Solaris RTP 150 which can reach a maximum temperature of 1300°C and a maximum gas flow of 900 sccm of nitrogen, oxygen and forming gas. The annealing recipe starts by purging the chamber with forming gas for 60 seconds at a rate of 900 sccm to remove oxygen from the chamber. Then, rapidly heating the chamber to the desired temperature at a ramp rate of 25°C per second and holding the temperature for a specified time. The RTA chamber is then cooled down by increasing the gas flow of N_2 to 900 sccm to extract the heat. The annealing was done using forming gas N_2/H_2 (volume ratio 98% : 2%) at a pressure of 600 sccm while pure N_2 was used to cool down the RTA chamber at a pressure of 900 sccm. Figure 4.6 shows an overview annealing process where AuGe/Ni/Au has been deposited using thermal evaporation on GaAs/$Al_xGa_{1-x}As$ heterostructure. The annealing recipe includes heating the chamber of RTA to 450°C for 80 seconds in N2/H2 gas and after annealing, an alloy of NiAuGe is formed which penetrates the heterostructure to contact the 2DEG.

4.9.6 The Transmission Line Method (TLM)

The transmission line method (TLM) has been used to calculate the contact resistance of metal contacts with the 2DEG [88–90]. The Ohmic contact should provide a linear relationship between current and voltage applied in a device. From a linear array of metal contacts with differently separated distances are defined along a stripe of the GaAs wafer. The resistance between subsequent Ohmics are measured when a voltage is applied to the contacts and the current is measured through the end of the contact. Assuming that contacts resistances

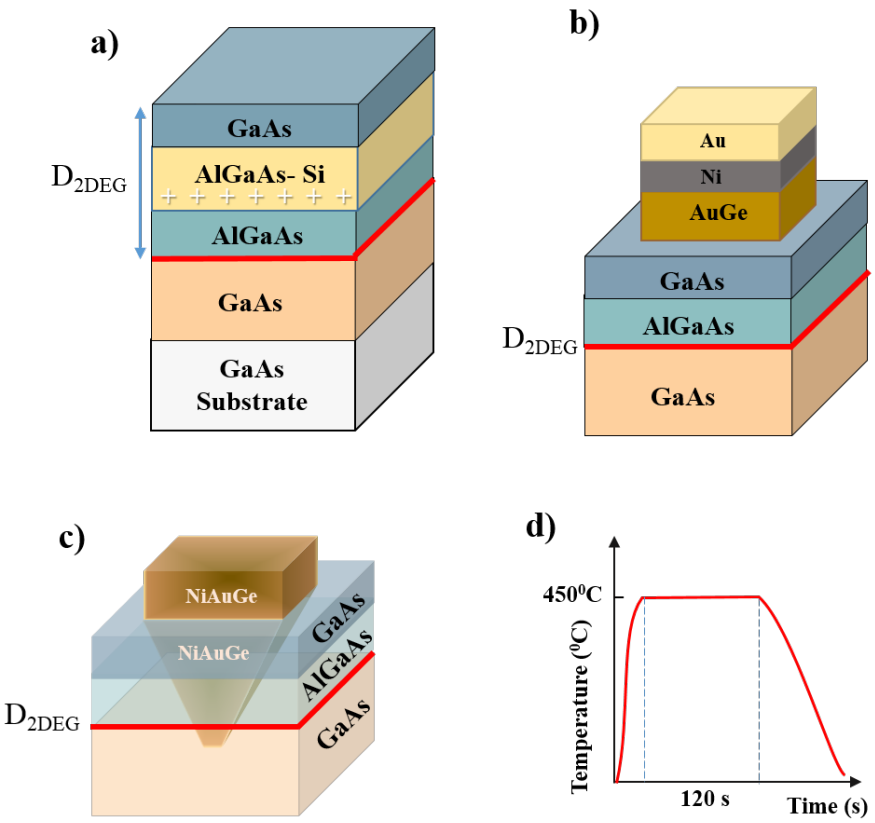

Figure 4.6: a) A schematic diagram of the layers of GaAs/$Al_xGa_{1-x}As$ heterostructures used on this study where the 2DEG forms at 90 nm below the surface. b) AuGe has been deposited followed by Ni followed by Au using thermal evaporation. c) After annealing, an alloy of NiAuGe is formed which penetrates the heterostructure to make contact with the 2DEG, d) The annealing recipe used by heating the RTA chamber to 450°C for 120 seconds in N2/H2 gas.

are the same for all the contact/semiconductor interfaces of the contacts on the mesa, the measured resistance R for a contact is given by

$$R = 2R_C + R_w + \frac{R_{sh}L}{W} \tag{4.4}$$

where R_{sh} is the sheet resistance of the semiconductor between the contacts, R_w is the resistance of the wires of the measuring cryostat, L is the distance between the contact pairs, W is the width of the semiconductor channel and R_c is the contact resistance. The contact resistance is the value that is considered important and R_c is counted twice since there are two interfaces for each contact pair. After subtracting the wire resistance, the measured resistance is a linear function of the distance d as shown in Fig 4.7 (b). The intercept of the line of the best fit at d=0 gives the value of the twice of the contact resistance R_c. The TLM mask used has a channel of 80 μm width. The Ohmic contacts had an area of 60 μm x 120 μm and separation distances of 60, 80, 105, 130, 180, 230, 380 and 980 μm. A schematic diagram of TLM array is shown 4.7(a). Two terminal measurement was used to measure the contact resistance between the consecutive pair of contacts. The series resistance of the wiring in the measurement setup was subtracted from the measured data. The series resistance was comparatively small compared to the resistance of the contacts ($\sim$ 1.0 Ω).

4.9.7 Optimising Temperature and Duration of Annealing

Optimising the annealing recipe has been done by varying the annealing temperatures and hold times. Ohmic contacts have been deposited on GaAs with the

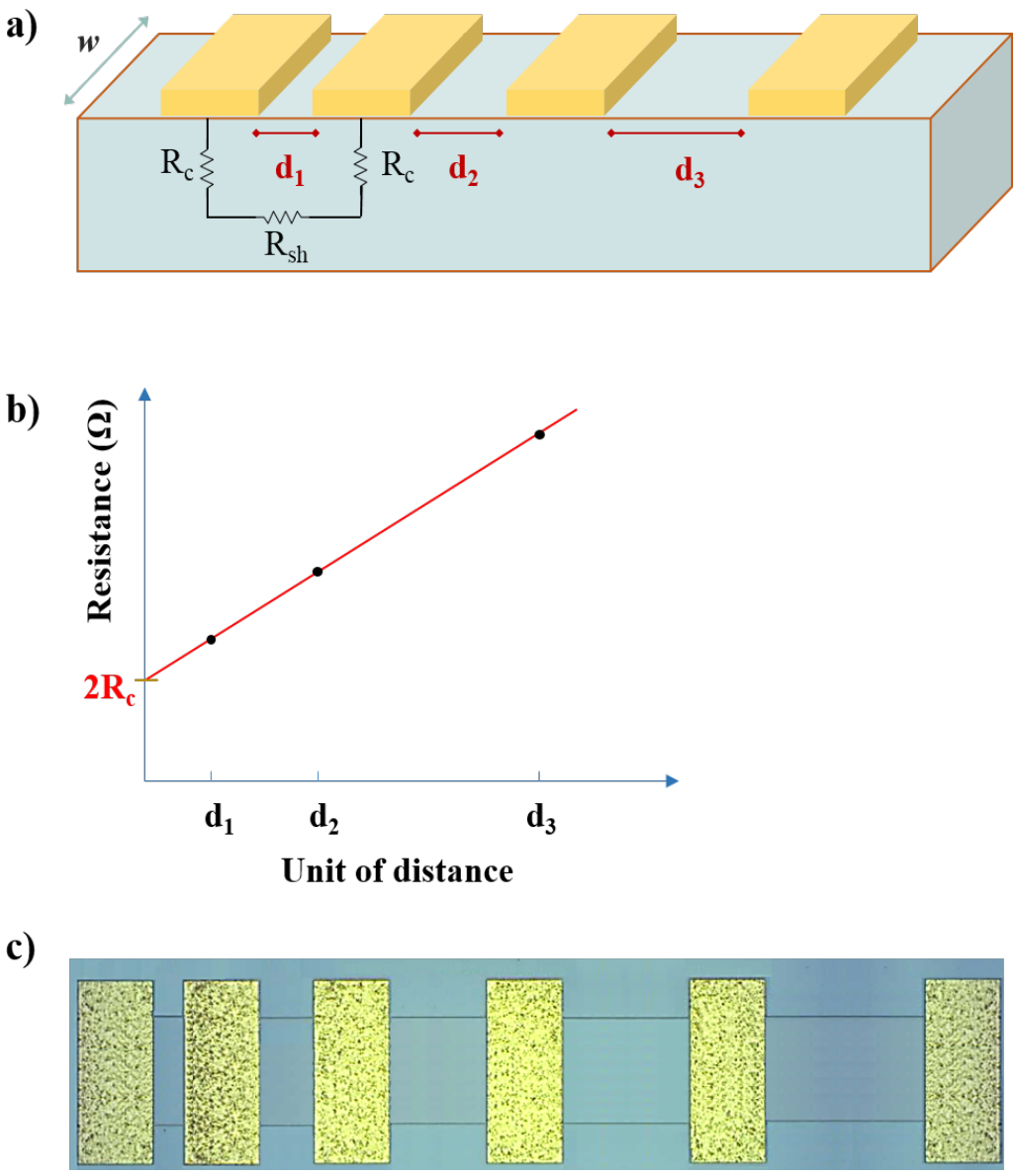

Figure 4.7: a) A schematic diagram of the linearly separated contact array used for TLM measurement. The yellow squares represents the contacts and blue represents the semiconductor channel where w is the width of the semiconductor channel and d_i is the distance between the contacts. R_c is the contact resistance and R_{sh} is the resistance arising from the semiconductor material. b) The plot of resistance versus contact separation distance d. The y-interception of the line of best fit to the data gives the value of twice the contact resistance R_c which was measured at 2.4 K. c) A microscopic image of a TLM sample.

following thickness AuGe (150 nm)/Ni (30 nm)/Au (150 nm). The annealing recipe starts by purging the chamber using forming gas for 60 seconds at a rate of 900 sccm to remove any oxygen from the chamber and then rapidly heating the chamber to various temperatures with a ramp rate of 25°C per second and holding the temperature for various times and then cooling down the chamber quickly by increasing the gas flow of N_2 to 900 sccm. The annealing was done using forming gas N_2/H_2 (volume ratio 98% : 2%) at a pressure of 600 sccm. The sample was then packaged in an LCC and placed in Helium-4 system with a base temperature of 2.4 K. The optimisation study was done using two wafers with different 2DEG depths, one was 90 nm and the other was 287 nm. Further details of each wafers are given in appendix A. Figure 4.8 shows the surface topography of the annealed Ohmic contacts. One may distinguish the annealing effects on the Ohmic contacts by comparing the images shown in figure 4.8 to determine if the Ohmic contact is an under annealed Ohmic or an over annealed contact or well annealed.

4.9.7.1 Shallow Wafer Optimisation Results

The shallow wafer used in the optimisation study is W475 and a growth sheet of the wafer is given in appendix A. The GaAs/$Al_xGa_{1-x}As$ heterostructure has 2DEG depth of 90 nm from the surface and a carrier density of 1.9×10^{11} cm^{-2} and electron mobility of 3.0×10^6 $cm^2V^{-1}s^{-1}$ in dark. The contacts resistance values were measured at 2.4 K. Looking through table I, the lowest resistance observed was 6.1 Ω for annealing duration of 80 seconds at 450°C. It is also noted that the lowest contact resistances occurs at 450°C for varying times. Another set of samples was annealed at 500°C and the results were not included as the

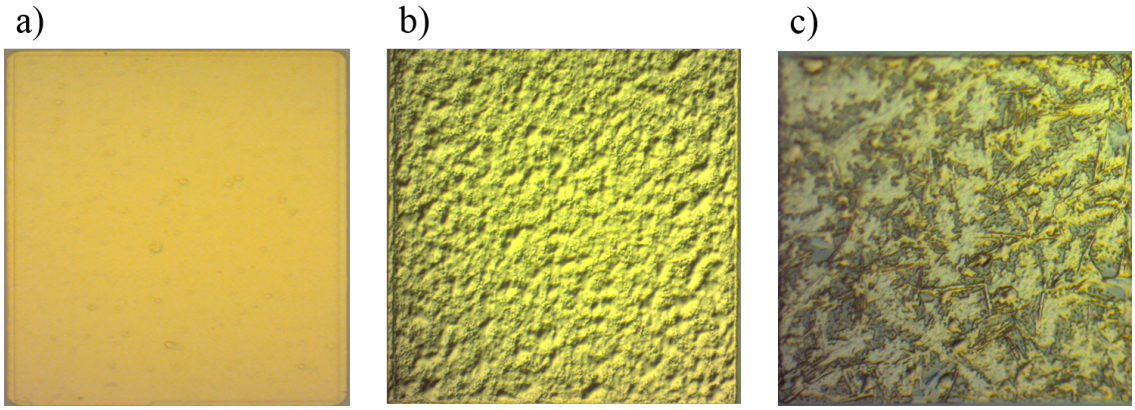

Figure 4.8: An optical pictures of several Ohmic contacts under different annealing conditions a) under annealed Ohmic contacts with a smooth uniform surface, b)shows a good annealed contact c) over annealed contacts where there are large grains present and surface morphology is poor.

contacts were conducting at room temperature however as the sample cooled down, the Ohmic contacts froze out and became unresponsive. Figure 4.9 shows the variation in resistance of Ohmic contacts for different annealing temperatures and durations where for each duration of time, the temperature has been varied.

Table I: The resistance of Ohmic contacts for different annealing tempertures and durations for shallow wafer W475.

Resistance ($\Omega \pm 0.5\ \Omega$)						
Temperature	60 s	80 s	100 s	120 s	180 s	200 s
400 °C	15.6	13.1	18.1	24.0	33.9	44.6
430 °C	8.7	7.4	11.8	19.0	29.7	36.3
450 °C	7.1	6.1	9.9	17.8	28.1	35.4
470 °C	13.1	11.2	15.3	24.0	29.8	40.1

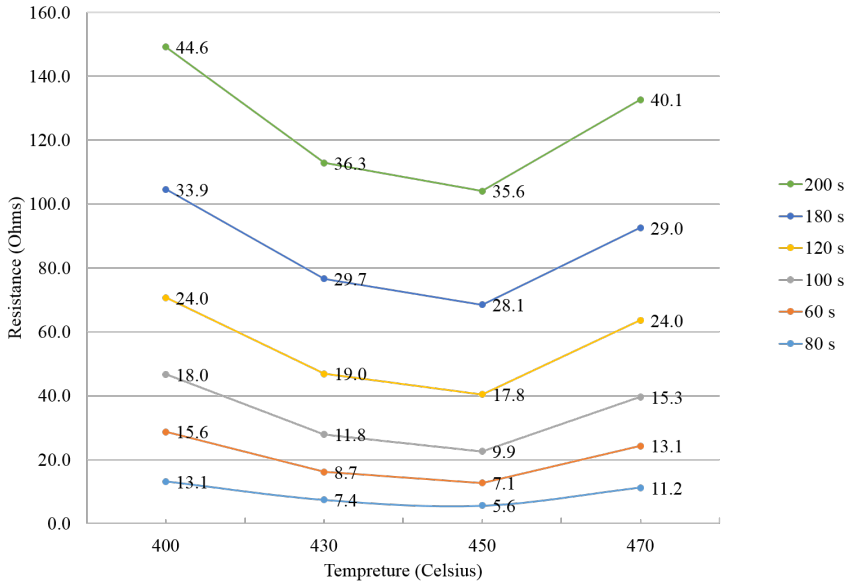

Figure 4.9: The variation of contact resistances, R_c, as a function of annealing temperatures for annealing times for wafer W475. The lowest contact resistances occurs at 450°C for varying times.

4.9.7.2 Deep Wafer Optimisation Results

The deep HEMT used in the optimisation study is W731 GaAs/$Al_xGa_{1-x}As$ heterostructure with a 2DEG depth of 287 nm from the surface and carrier density was 4.5×10^{10} cm^{-2} and electron mobility was 1.2×10^6 $cm^2V^{-1}s^{-1}$ in the dark. A growth sheet of this wafer (W731) has been included in Appendix A. The resistance values were measured at 2.4 K. Looking through table II, the lowest resistance obtained was 27.1 Ω for an annealing duration of 200 seconds at 450°C. It is also noted that the lowest contact resistances occurs at 450°C for varying times too.

The results of samples annealed at 500 and 510°C were not included as the contacts had high contact resistance at room temperature and as the samples

were cooled down, the Ohmic contacts froze out and became unresponsive; this may be due to metal spiking and destroying the 2DEG underneath [82]. Samples annealed for a short duration of 60 seconds for various temperatures also froze out during cool down as the NiAuGe did not penetrate deep enough to make electrical contact with the 2DEG. Figure 4.10 shows the variation in the contact resistance of the Ohmic contacts for various annealing temperatures and durations. For every specific duration of time, the temperature has been varied.

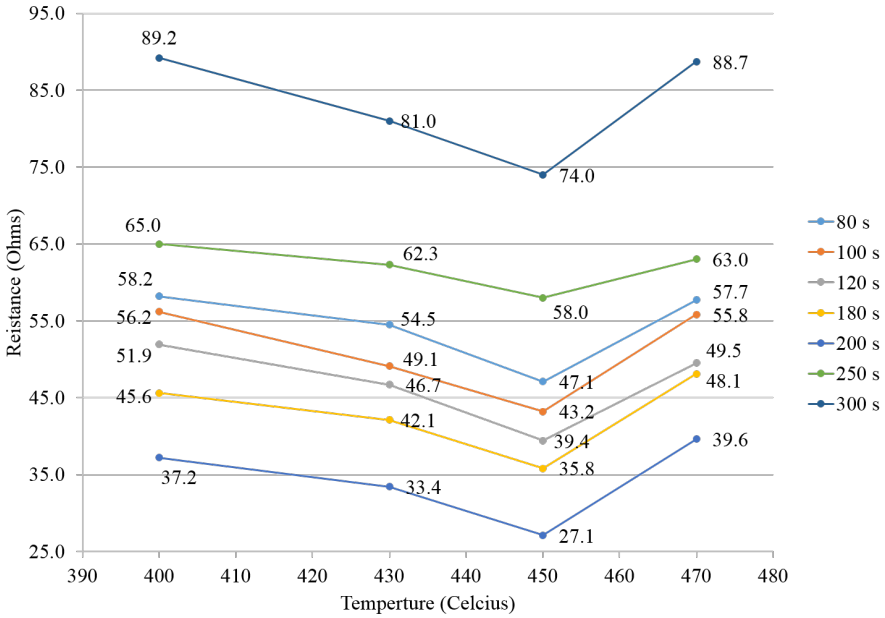

Figure 4.10: A graph shows the variation of contact resistances, R_c, as a function of annealing temperatures for annealing times for wafer W731 measured at 2.4 K. The lowest contact resistances occurs at 450°C for 200 seconds.

Table II: The resistance of Ohmic contacts for different annealing temperatures and durations for deep wafer W731.

Resistance (Ω ± 4.0 Ω)							
Temperature	80 s	100 s	120 s	180 s	200 s	250 s	300 s
400 °C	58.2	56.2	51.9	45.6	37.2	65.0	89.2
430 °C	54.5	49.1	46.7	42.1	33.4	62.3	81.0
450 °C	47.1	43.2	39.4	35.8	27.1	58.0	74.0
470 °C	57.7	55.8	49.5	48.1	39.6	63.0	88.7

4.9.8 Influence of Ni Layer in Ohmic Contacts

Ni layer is beneficial in improving the morphology of the contacts and in the diffusion of the metal into the GaAs. However increasing the Ni thicknesses beyond the optimum point leads to higher Ohmic contact resistance and the excess Ni might unreact forming a ferromagnetic structures in the contact. A study was performed with varying Ni thickness in the Ohmic contacts. The recipe was AuGe (150 nm)/Ni (x nm)/Au (150 nm), x = 15, 20, 25, 30, 35, 40, 45, 50 nm and the sample was annealed at 450°C for 80 seconds for shallow wafer W475 and 450°C for 200 seconds for the deep wafer W731. The Ohmic contacts with a Ni-layer thickness of 25-30 nm resulted in the lowest contact resistance among the samples studied. A Dektak thickness profiler was used to measure the roughness of the surface of contact and the roughness of contacts was found to reduce by increasing Ni thickness.

4.9.8.1 Shallow Wafer Optimisation Results

Table III shows the effect of varying the thickness of Ni on the contact resistance, R_C. The resistance starts decreasing as the thickness of Ni is increased until it reaches a minimum value of 7.1 Ω when the Ni thickness is 35 nm. When

Ni thickness is increased beyond 35 nm, the resistance was found to increase monotonically.

Table III: The resistance of Ohmic contacts for different thicknesses of Ni for shallow wafer W475.

Wafer	$D_{2DEG},\ nm$	$n,\ cm^{-2}$	$\mu,\ cm^2/V.s$	AuGe/Ni/Au(nm)	$R_c, \Omega \pm 0.5\Omega$
W475	90	1.9×10^{11}	3.0×10^6	150/15/150	16.1
W475	90	1.9×10^{11}	3.0×10^6	150/20/150	10.3
W475	90	1.9×10^{11}	3.0×10^6	150/25/150	8.0
W475	90	1.9×10^{11}	3.0×10^6	150/30/150	7.8
W475	90	1.9×10^{11}	3.0×10^6	150/35/150	7.1
W475	90	1.9×10^{11}	3.0×10^6	150/40/150	13
W475	90	1.9×10^{11}	3.0×10^6	150/45/150	17.3
W475	90	1.9×10^{11}	3.0×10^6	150/50/150	30.3

4.9.8.2 Deep Wafer Optimisation Results

Table IV shows the effect of varying the thickness of Ni on the contact resistance R_C using wafer W731. The resistance starts decreasing as the thickness of Ni is increased until it reaches a minimum value of 24.4 Ω ± 3.0 Ω when the Ni thickness is 35 nm. When Ni thickness is increased beyond 35 nm, the contact resistance was found to increase as shown in figure 4.11.

Table IV: The resistance of Ohmic contacts for different thicknesses of Ni for deep wafer W731.

Wafer	$D_{2DEG},\ nm$	$n,\ cm^{-2}$	$\mu,\ cm^2/V.s$	AuGe/Ni/Au, nm	$R_c, \Omega \pm 3.0\Omega$
W731	287	4.5×10^{10}	1.2×10^6	150/20/150	38.9
W731	287	4.5×10^{10}	1.2×10^6	150/25/150	35.9
W731	287	4.5×10^{10}	1.2×10^6	150/30/150	27.1
W731	287	4.5×10^{10}	1.2×10^6	150/35/150	25.4
W731	287	4.5×10^{10}	1.2×10^6	150/40/150	31
W731	287	4.5×10^{10}	1.2×10^6	150/45/150	48
W731	287	4.5×10^{10}	1.2×10^6	150/50/150	64.3

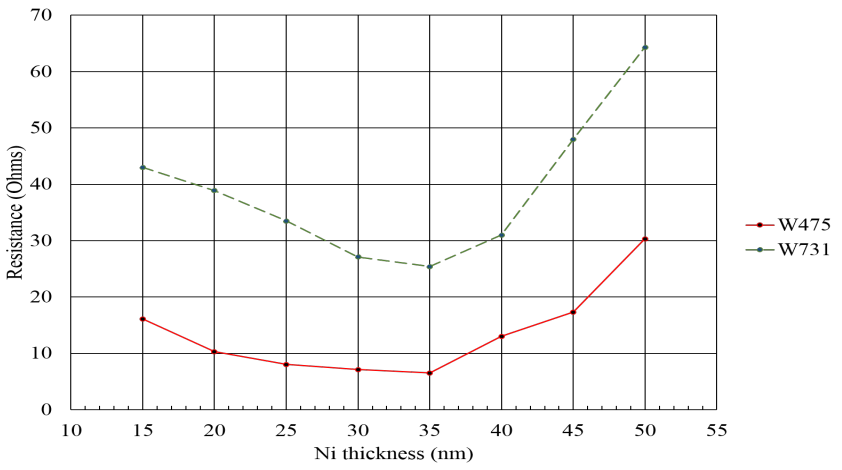

Figure 4.11: The contact resistances, R_c, for wafer W731 and W475 as a function of the Ni layer thickness measured at 2.4 K. The lowest contact resistances occurs for a Ni thickness of 35 nm for both wafers.

4.9.9 Influence of AuGe Layer in Ohmic Contacts

The AuGe layer is beneficial in making low resistance Ohmic contacts as AuGe diffuses into GaAs and makes high doping levels which makes tunnelling through

the contacts possible. However increasing the AuGe thickness beyond the optimum point may lead to higher Ohmic contact resistance as the excess AuGe might not react with Ni leading to balling up of the contact. A study was performed with varying AuGe thickness in the Ohmic contacts. The recipe was AuGe (x nm)/Ni (35 nm)/Au (150 nm), x = 75, 100, 125, 150, 175, 200, 225 nm and the sample was annealed at 450°C for 80 seconds for shallow wafer (W475) and 450°C for 200 seconds for the deep wafer (W731).

4.9.9.1 Shallow wafer optimisation Results

Table V shows the effect of varying the thickness of AuGe on the contact resistance, R_C, using wafer W475. The resistance starts decreasing as the thickness of AuGe is increased until it reaches a minimum value of 5.4 Ω when the AuGe thickness is 175 nm. When the AuGe thickness is increased beyond 175 nm, the resistance starts to increase but at a slower rate compare to the study when Ni was varied, [see figure 4.11 and figure 4.12].

Table V: The resistance of Ohmic contacts for different thicknesses of AuGe for shallow wafer W475.

Wafer	$D_{2DEG},\ nm$	$n,\ cm^{-2}$	$\mu,\ cm^2/Vs$	AuGe/Ni/Au, nm	$R_c, \Omega \pm 0.5\Omega$
W475	90	1.9×10^{11}	3.0×10^6	75/35/150	15.6
W475	90	1.9×10^{11}	3.0×10^6	100/35/150	12.3
W475	90	1.9×10^{11}	3.0×10^6	125/35/150	8.1
W475	90	1.9×10^{11}	3.0×10^6	150/35/150	6.5
W475	90	1.9×10^{11}	3.0×10^6	175/35/150	5.4
W475	90	1.9×10^{11}	3.0×10^6	200/35/150	7.3
W475	90	1.9×10^{11}	3.0×10^6	225/35/150	10.7

4.9.9.2 Deep wafer optimisation Results

Table VI shows the effect of varying the thickness of AuGe on the contact resistance R_C using wafer W731. The resistance starts decreasing as the thickness of AuGe is increased until it reaches a minimum value of 22.3 Ω when the AuGe thickness is 175 nm. When AuGe thickness is increased beyond 175 nm, the resistance start increasing.

Table VI: The resistance of Ohmic contacts for different thicknesses of AuGe for deep wafer W731.

Wafer	$D_{2DEG},\ nm$	$n,\ cm^{-2}$	$\mu,\ cm^2/Vs$	AuGe/Ni/Au, nm	$R_c, \Omega \pm 3.0\Omega$
W731	287	4.5×10^{10}	1.2×10^6	75/35/150	40.2
W731	287	4.5×10^{10}	1.2×10^6	100/35/150	35.6
W731	287	4.5×10^{10}	1.2×10^6	125/35/150	32.5
W731	287	4.5×10^{10}	1.2×10^6	150/35/150	25.4
W731	287	4.5×10^{10}	1.2×10^6	175/35/150	22.3
W731	287	4.5×10^{10}	1.2×10^6	200/35/150	28.1
W731	287	4.5×10^{10}	1.2×10^6	225/35/150	30.5

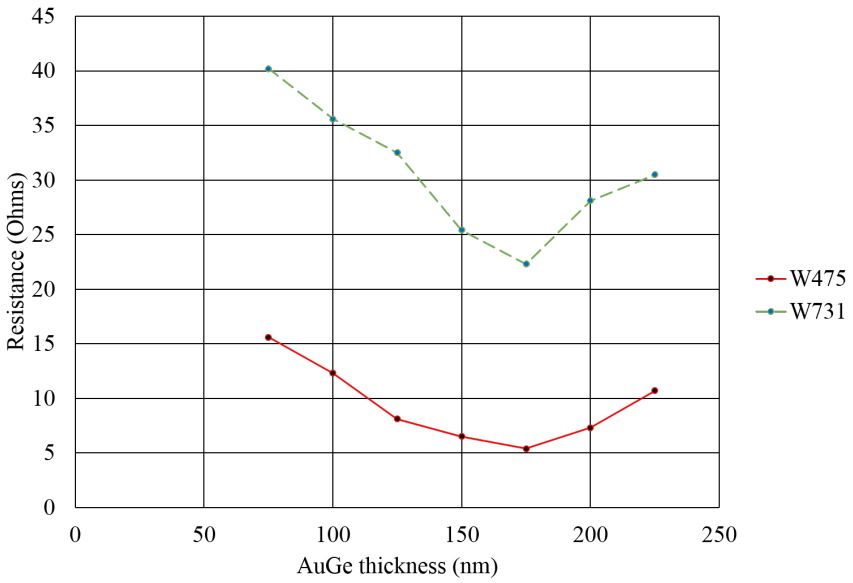

Figure 4.12: The contact resistances, R_c, for wafer W731 and W475 as a function of AuGe thickness. The lowest contact resistances occurs at a AuGe thickness of 175 nm for both wafers.

4.9.10 Initial Layer of Ni in Ohmic Contacts

Valeille *et al.* have reported that having an initial layer of Ni before depositing standard NiAuGe Ohmic contacts can improve the yield and lower the contact resistance [91, 92]. A similar study was done to investigate the effect of adding an initial layer of Ni to the contact resistance, R_c. The recipe was Ni (x nm)/ AuGe (175 nm)/Ni (35 nm)/Au (150 nm), x = 2, 3, 5, 6, 7 nm and the samples were annealed at 450°C for 80 seconds for shallow wafer (W475) and 450°C for 200 seconds for the deep wafer (W731). Adding an initial layer of Ni (2-5 nm) to the Ohmic contacts has decreased its value but only by a small margin of less than 1 Ω ±0.5Ω.

4.9.10.1 Shallow Wafer Optimisation Results

Table VII shows the effect of adding an initial layer of Ni and effect of varying its thickness on the contact resistance, R_C, using wafer W475. The resistance values decrease slightly when adding a layer of Ni of thickness 2-5 nm however beyond that the contact resistance started increasing. A minimum resistance value of 4.9 Ω is achieved when the Ni thickness is 4 nm. When Ni thickness is increased beyond 5 nm, the contact resistance was found to increase.

Table VII: The resistance of Ohmic contacts for different thicknesses of an additional initial layer Ni for shallow wafer W475.

Wafer	$D_{2DEG},\ nm$	$n,\ cm^{-2}$	$\mu,\ cm^2/Vs$	Ni/AuGe/Ni/Au, nm	$R_c, \Omega \pm 0.4\Omega$
W475	90	1.9×10^{11}	3.0×10^6	2/175/35/150	5.4
W475	90	1.9×10^{11}	3.0×10^6	3/175/35/150	5.2
W475	90	1.9×10^{11}	3.0×10^6	4/175/35/150	4.5
W475	90	1.9×10^{11}	3.0×10^6	5/175/35/150	4.9
W475	90	1.9×10^{11}	3.0×10^6	6/175/35/150	6.1
W475	90	1.9×10^{11}	3.0×10^6	7/175/35/150	7.3

4.9.10.2 Deep Wafer Optimisation Results

Table VIII shows the effect of adding an initial layer of Ni and the effect of varying its thickness on the contact resistance, R_C, using wafer W731. The resistance values decrease slightly when adding a layer of Ni of thickness 2-5 nm however beyond that the contact resistance started increasing. A minimum resistance value of 20.6 Ω is achieved when the Ni thickness is 4 nm. When Ni thickness is increased beyond 4 nm, the contact resistance started increasing. Figure 4.13 shows the effect of increasing the Ni thickness on the Ohmic contact.

Table VIII: The resistance of Ohmic contacts for different thicknesses of adding an intial layer Ni for deep wafer W731.

Wafer	D_{2DEG}, nm	n, cm^{-2}	μ, cm^2/Vs	Ni/AuGe/Ni/Au, nm	$R_c, \Omega \pm 3.0\Omega$
W731	287	4.5×10^{10}	1.2×10^6	2/175/35/150	22.2
W731	287	4.5×10^{10}	1.2×10^6	3/175/35/150	21.3
W731	287	4.5×10^{10}	1.2×10^6	4/125/35/150	20.6
W731	287	4.5×10^{10}	1.2×10^6	5/150/35/150	21.4
W731	287	4.5×10^{10}	1.2×10^6	6/175/35/150	23.1
W731	287	4.5×10^{10}	1.2×10^6	7/175/35/150	27.2

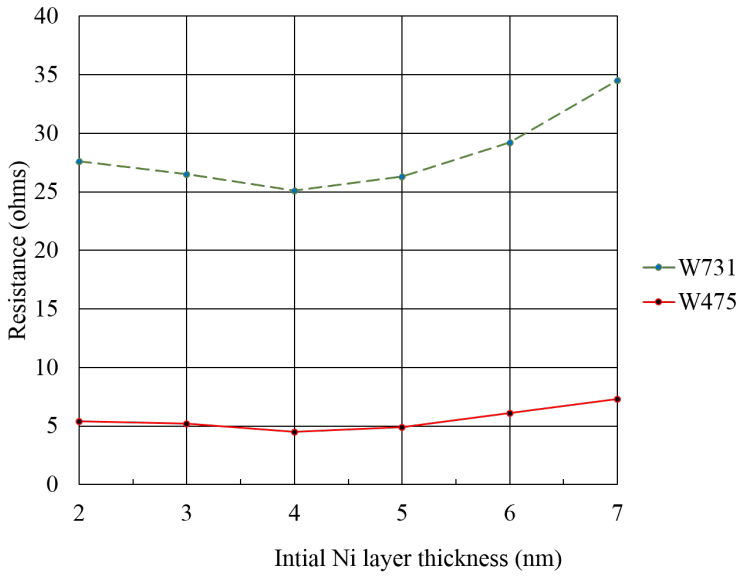

Figure 4.13: The variation of the contact resistances, R_c, for wafer W731 and W475 as a function of the initial Ni thickness. The lowest contact resistances occurs at 4 nm for both the wafers.

4.9.11 Surface Treatment of GaAs

A low resistance contact can be achieved provided that there is a clean interface between the semiconductor and the metal. Therefore, the oxide layer that forms on GaAs has to removed prior to metal deposition. A significant amount of work has been reported on surface passivation and oxide removal of GaAs [93, 94]. Wet etching is commonly used to remove the native oxide and contaminates from III-V materials. Upon exposure to atmosphere air, the oxide starts growing immediately on the surface. When loading the sample in the evaporator, it will be exposed to air and a mono-layer of oxide can grow on the sample and oxide growth is inevitable if wet etching is used. The oxide removal should be done in an oxygen-free environment like a glove box or using plasma etching like in-situ Ar-milling to remove the oxide before metal deposition. It ensures that the oxide layer is removed and it is important to optimise this process as it can etch through the GaAs. Wet etching was used to remove the oxide layer as the thermal evaporator lacked a plasma etching facilities. Several solutions were used to remove the oxide layer like HCl, NH_4OH, $(NH_4)_2S$ and their effect on the contact resistance was examined. The sample was then loaded in the evaporator quickly to avoid oxide regrowth. The ohmic contacts were evaporated with the following recipe of Ni/AuGe/Ni/Au of thickness 4/175/35/150 nm and the shallow wafer W475 was annealed at 450°C for 80 seconds and the deep wafer W731 was annealed at 450°C for 200 seconds.

4.9.11.1 Hydrochloric acid

Removing the oxide using HCl tends to react with the As on the GaAs surface and leaves a surface rich in As [95]. The sample was dipped in 5:40 HCl/H_2O solution for 10 seconds followed by a rinse in a DI water bath. The Ohmic contact, R_C, showed a value of 4.5 Ω for wafer W475 and a value of 20.6 Ω for wafer W731.

4.9.11.2 Ammonium Hydroxide

NH_4OH solution can be used to remove the oxide layer from GaAs surface and it can also be used for removing organic and metallic impurities. The sample was dipped in 1:9 NH_4OH/H_2O solution for 10 seconds followed by rinse in DI water bath. The benefits of using NH_4OH are also that it removes metal ion contaminates, removing the oxide layer and its saponification effects to remove oil and greases contaminates. NH_4OH can also keep a stoichiometric concentration at the GaAs surface (As/Ga=0.99) [96]. The Ohmic contact, R_C, showed a value of 4.2 Ω for wafer W475 and a value of 20.1 Ω for wafer W731. The contact resistance values are very similar to the samples treated with HCl.

4.9.11.3 Ammonium Sulphide

Ammonium sulphide $(NH_4)_2S$ can also be used to remove the native oxide layer [97–99]. The chemical used is $(NH_4)_2S$ 20% ammonium sulphide solution and sulphur powder was added to form ammonium polysulphide solution. Adding sulphur powder increases the passivation capacity and decreases the pH of the solution. The samples were treated for 5 minutes in the solution at 40°C as any temperature beyond that will degrade the solution. The sample is then rinsed in

DI water for a further 5 minutes and loaded quickly in the thermal evaporator. The Ohmic contact, R_C, showed a value of 4.4 $\pm$ 0.5 Ω for wafer W475 and the contact resistance values are similar to the samples treated with HCl and NH_4OH.

4.9.12 SEM of Ohmic Contacts

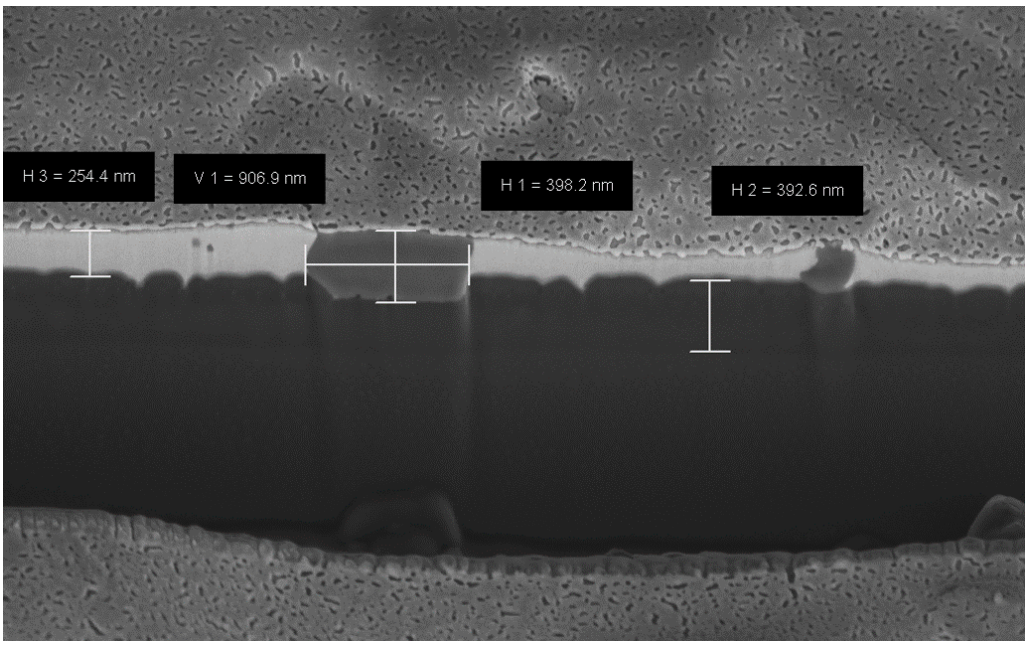

Figure 4.14: An SEM image of the cross section of good annealed ohmic contacts etched using Ga focused-ion beam.

To have a closer look at the ohmic contacts, a ZEISS CrossBeam Focused Ion Beam (FIB) was used to etch away a rectangular box at the interface between the contact and Mesa using a Ga ion source. Cross sectional images of the contacts were taken using SEM and are shown in figure 4.14. The SEM image shows that there is spike formation which penetrates deep into the substrate. Using EDS analysis, the dark areas are Ni and Ge rich while the white areas are Au rich. The grains are smaller than 1 μm. In addition, the GaAs/AlGaAs interface under

the contact is usually consumed during the annealing process and can be seen in the cross sectional image.

4.10 Electron Beam Lithography

Electron beam lithography (EBL) is a a method of patterning a design using a focused electron beam on a surface covered with electron sensitive resist. The EBL systems have a resolution of sub 10 nm as the election de Broglie wavelength is much smaller than that of ultra-violet light used in the optical lithography machines. EBL sends a beam of electrons at an electron sensitive resist such as poly-methyl-methacrylate (PMMA) which breaks the polymer chains. Also, the advantage of using EBL is that there is no mask required to pattern the design on the e-beam resist. However, its disadvantage is the long times taken to write large patterns. EBL machines were designed using scanning electron microscopes (SEM) combined with a design generator and beam blanker to control which areas are to be exposed. EBL machines have more control over the dosage of the electron beam. In an EBL system, the electron beam is generated by an electron gun and then passes through series of condenser and deflector lenses to focus the electron beam. The deflection of the beam is limited to a fixed area called the write field alignment. If the designs to be patterned can not fit into a single write field, the pattern is usually divided into a grid of several write field adjacent to each other and is exposed sequentially. A precise field alignment is necessary to avoid any stitching errors since there is not perfect matching between adjacent write fields. Figure 4.15 shows the stitching process of the EBL as the design is exposed sequentially in a grid of write fields. The stage has a highly precise

control as it is controlled by laser-interferometric position system.

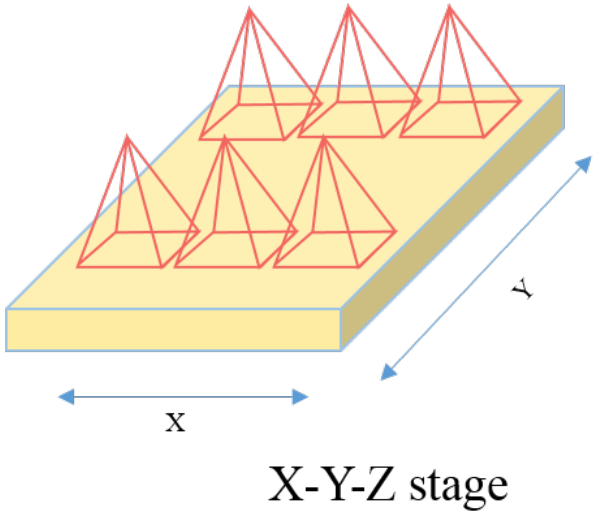

Figure 4.15: A schematic diagram of the write fields stitching process of a large design where it is exposed in a series of grid of write fields.

Electrons exhibit two types of scattering when exposing the sample which are forward and back-scattering. Forward scattering occurs due to angle deflection of electrons when passing through the resist which causes the beam to widen and thus the pattern gets widened too. Back-scattering happens after the electrons pass through the resist, penetrates the sample and bounce back into the resist. Scattering induce proximity effects where the exposure of an area is effected by the exposure of the surrounding area causing distortion in the pattern and overexposure. Scattering can be reduced by increasing the energy of the beam which leads to scattering occurring deep in the sample and thus reducing the scattering significantly and allowing finer features to be patterned. The highest energy beam, 30 kV, was used in pattering the design which is the highest possible setting for the EBL machine used in this research a Raith-150.

The samples are coated with PPMA 950K-A4 which is produced by Micro Chem. PPMA-950K-A4 contains anisole with 4% ploy-methyl-methacrylate with a molecular weight of 950K. PMMA is a widely used resist with a resolution of 10 nm and weak sensitivity to light. The chip is spun at 500 rpm for 5 seconds and then 6000 rpm for 45 seconds. The resist is baked for 2 minutes at 180°C. The recipe leads to a resist of 300 nm thick which is enough for metal deposition. The EBL machine was set to 30 kV electron beam and 20 μm diameter aperture to pattern the design. Smaller apertures make a smaller depth of field which leads to higher resolution and smaller current which increases exposure time. For these setting, the optimal dose was tested to be 300 $\mu C/cm^2$ for areas and 900 $\mu C/cm^2$ for fine lines. Different parameters and setting needs to be optimised to ensure high resolution. These settings are the aperture alignment, the stigmation of the beam, working distance and write field alignment. After the sample is exposed, it is dipped in a developer which is 1:3 methyl isobutyl ketone(MIBK): IPA. The sample is gently agitated for 60 seconds to develop the pattern followed by a dip in IPA for 15 seconds to stop further developing.

4.10.1 Bi-layer Process

For thick metal depositions, a double layer of PMMA 950K-A4 is spun to ensure proper lift-off. The first layer of PMMA 950K-A4 is spun and baked at 180°C for 2 minutes; followed by spinning of the second layer of PMMA 950K-A4 and baking the sample again for a further 2 minutes. For the bi-layer, the developing time increases from 60 seconds to 90 seconds to ensure that the resist has been fully developed.

For metal depositions of gates with large feature size, it can be done by creating an undercut profile to improve lift-off using a double-layer PMMA. In the bilayer PMMA process, a layer of PMMA (495K-A2) is spun on the sample first at 6000 rpm for 45 seconds and then baked for 2 minutes at 180°C. Another layer of PMMA 950K-A4 is spun on top pf the first layer at 6000 rpm and baked for 2 minutes at 180°C. PMMA 495K-A2 is more sensitive to the electron beam than PMMA 950K-A4. When the sample is exposed and developed, the lower layer (PMMA 495K-A2) will be more undercut than the upper layer (PMMA 950K-A4).

4.10.2 Cross-linking PMMA

The electron beam when exposed to PMMA breaks up the polymer chains which means the PMMA is more soluble in solvent and can be developed. However, this behaviour does not extend to an infinite dose and at higher dosage, the PMMA starts cross linking and it becomes less soluble in solvents [100, 101]. An optimisation process was done to establish the optimum electron beam dosage needed for cross-linking by measuring the thickness of cross-linked PMMA after dissolving it in acetone; a similar process was first done by Teh *et al.* [102]. To reduce the exposure time to a minimum, a large aperture of 120 μm and 10 kV accelerating voltage was used which provides the maximum amount of current. A double layer of PMMA 950K-A4 has been used and spun at 6000 rpm for 45 seconds and baked for 4 minutes at 170°C. The bilayer PMMA resist gives a thickness of 350 nm. The bilayer resist was cross linked by the electron beam at different electron dosage from 4 to 340 $\mu C/m^2$. The square boxes of

10 μm x 10 μm were cross linked and then the sample was dipped in acetone or 1165 solution for 10 minutes to remove the resist. The cross linked features are inspected optically and its thickness is measured using a Dektak surface profiler. From figure 4.16, the dosage needed for full cross linking is around 200 $\mu C/m^2$ and the minimum dosage required for cross linking is 40 $\mu C/m^2$. Partial cross linking occur when the dosage is between 40 $\mu C/m^2$ and 200 $\mu C/m^2$. When the PMMA is fully cross linked, the thickness of the PMMA decreased by a factor of 0.8 . Figure 4.17 shows a top-gate deposited over cross-linked PMMA which acts as a dielectric.

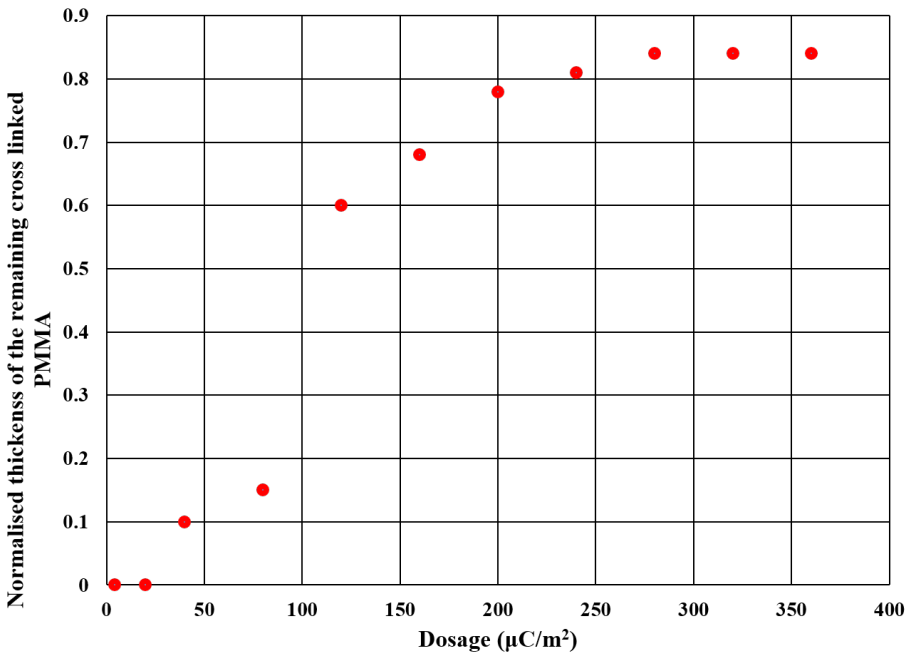

Figure 4.16: Normalised thickness of cross-linked PMMA versus the electron beam dosage.

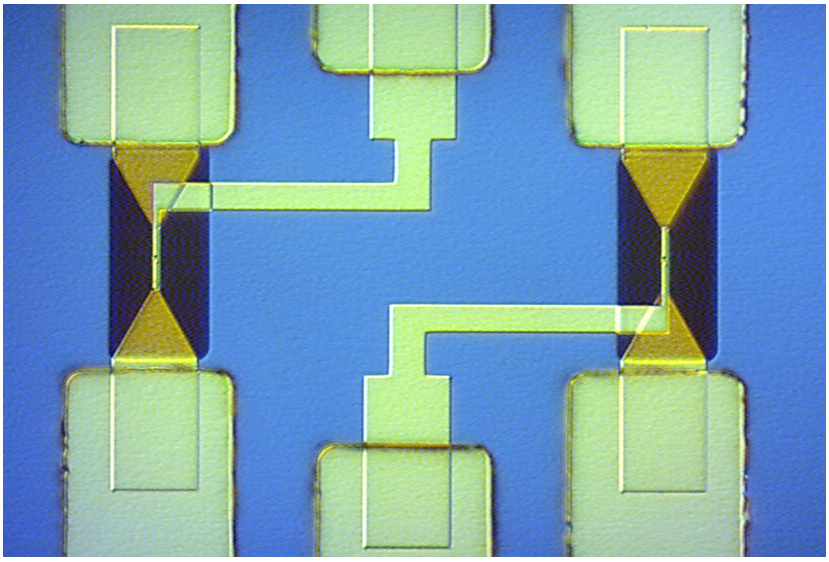

Figure 4.17: A microscopic picture of a top-gated device with cross-linked PMMA

4.11 Optical gates

Optical gates are used to connect the gates drawn by EBL to large bonding pads. The fabrication process of optical gates includes the bi-layer of LOR-3A and Shipley 1818 optical resist. The LOR-3A is spun at 500 rpm for 5 seconds and then 7000 rpm for 45 seconds and baked for 10 minutes at 170°C, followed by, spinning the S1818 resist at 500 rpm for 5 seconds and then 7000 rpm for 45 seconds and baked for 60 seconds at 115° C. The sample is developed in MF-319 developer for 60 seconds and the sample is then placed in an O_2 plasma asher for 1 minute. An oxide removal treatment of the sample is crucial for the Ti/Au to stick on the surface otherwise the gates will peel off during lift-off or bonding. E-beam evaporator is used to evaporate Ti/Au (20 nm/120 nm) onto the device which provides a clean and smooth surface. The sample holder is rotated while evaporating to avoid the creation of lilly pads and discontinuities in the gates.

Figure 4.18 shows optical gates deposited on GaAs where it connects the EBL gates to large pads for bonding, usually 100 μm x 100 μm.

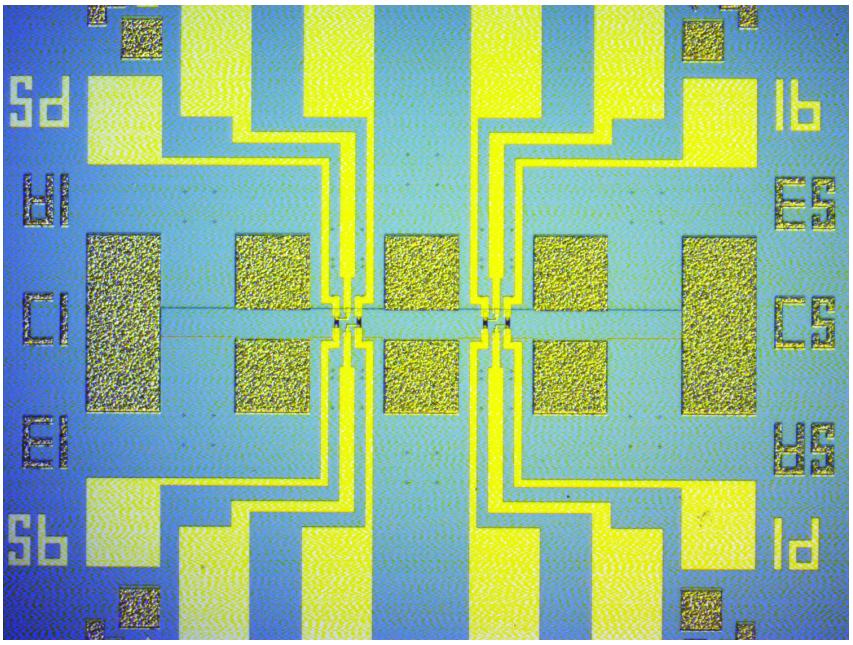

Figure 4.18: Top-gated Device with evaporated Ti/Au optical gates.

4.12 Back gate

In this section, a method for reproducing thinning of the sample to 50 μm using wet etching and the subsequent ultrasonic bonding can be used to make contact to gates on either side of the sample is presented. The wafer is thinned down from 550 μm to 100-50 μm to effectively reduce the need to apply large negative voltages using a back gate to modulate the density of electrons in the 2DEG [103]. Figure 4.19 shows the schematic of the steps used to fabricate the back gate. The GaAs wafer had an initial thickness of 550 μm before etching. After finishing the topside fabrication of Ohmics and Schottky split gates, a photore-

sist (SPR-220) layer of thickness 10 μm was spun on the topside of the chip to protect the devices from wet etching. Then, the GaAs chip was mounted topside down on a thin glass slide and the sample was then baked at 115°C for 3 mins for the photoresist to harden (Figure 4.19 (a)). The SPR-220 photoresist is resistant to the acid peroxide etch solution and the photoresist can be removed if the chip is soaked in acetone (Figure 4.19 (b)). The thinning of the GaAs chip was then carried out using a sulphuric acid/peroxide solution 1:1:9 H_2SO_4: H_2O: H_2O_2. With an optimised etching rate of 15 μm/min, the chip was etched down to a thickness of 50-100 μm (Figure 4.19 (c)). The thickness of the chip was measured using a Dektak thickness profilometer. The chip was then loaded in an e-beam evaporator to deposit Ti/Au (30 nm/120 nm) for the back gate metallisation. After the back gate metallisation, the chip was placed in acetone to dissolve away the photoresist (Figure 4.19 (d)). The chip was then mounted with Ti/Au metallisation facing down on a non-magnetic leadless chip carrier (LCC) using silver epoxy to provide electrical contact and also mechanical support to the thinned chip (Figure 4.19 (e)). Gold wire bonds were then made to the contact pads on the topside and to the back gate via the silver conducting epoxy using conventional ultrasonic bonder. Figure 4.20 shows scanning electron microscopy images for a comparison between un-etched (550 μm thick chip) and etched chip (50 μm thick) with a back gate. Figure 4.21 shows scanning electron microscopy images of two packaged devices: (top) an etched split-gate device with a back gate, mounted using conducting silver epoxy; (bottom) un-etched split-gate device without a back gate where a non-conductive Ge-varnish was used to glue the chip to the base of LCC.

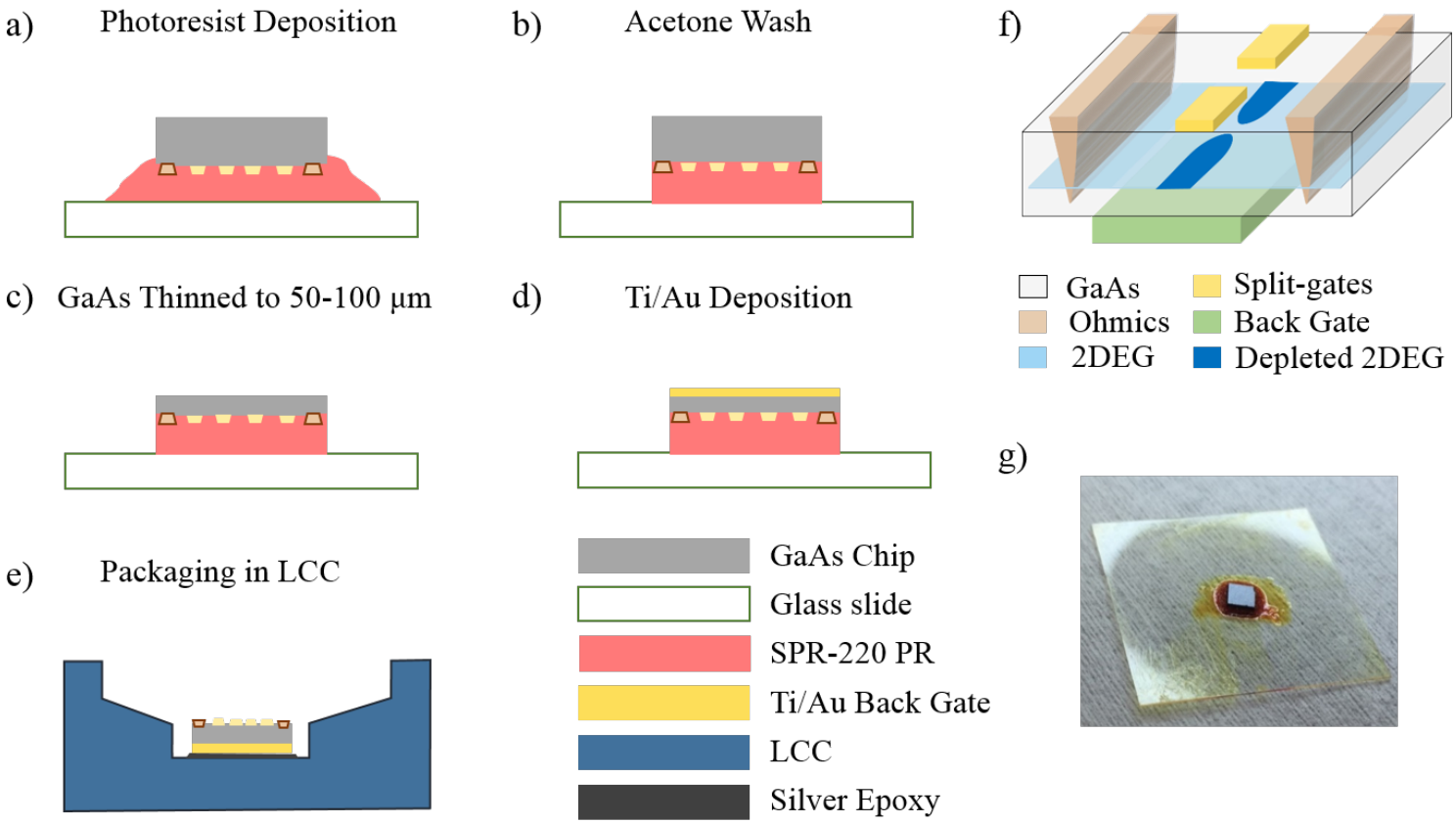

Figure 4.19: A schematic diagram showing the fabrication steps for adding a back gate to a GaAs sample. a) a positive photoresist is spun coated on the topside of the GaAs chip containing a fabricated 1D device which is then mounted with topside coated photoresist facing down on a thin glass slide, b) acetone is used to wash-off any excess photoresist on the backside and corners, c) thinning down the chip to 50-100 μm using the wet-etching technique, d) a uniform metal layer of Ti/Au is deposited to form a back gate, e) the processed chip with a back gate is packaged in an LCC using conductive silver epoxy, f) a schematic diagram of the 1D device showing a pair of split gate, Ohmics contacts for source and drain, a back gates for tuning the carrier density in the 1D quantum wire and g) a photograph of the chip after thinning down to 50-100 μm.

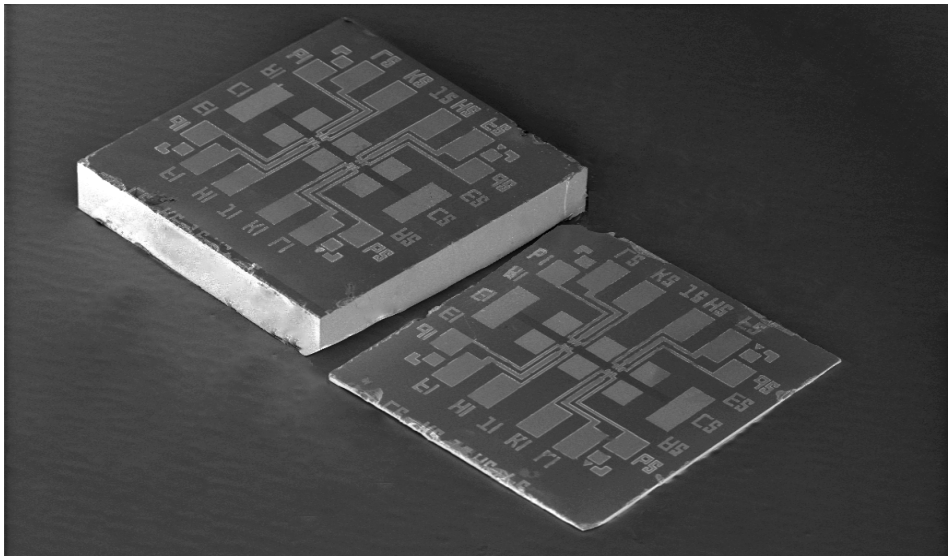

Figure 4.20: A scanning electron microscopy image of the fabricated device which shows a chip before etching (top) with a thickness of 550 μm and after etching to a thickness of 50 μm (bottom).

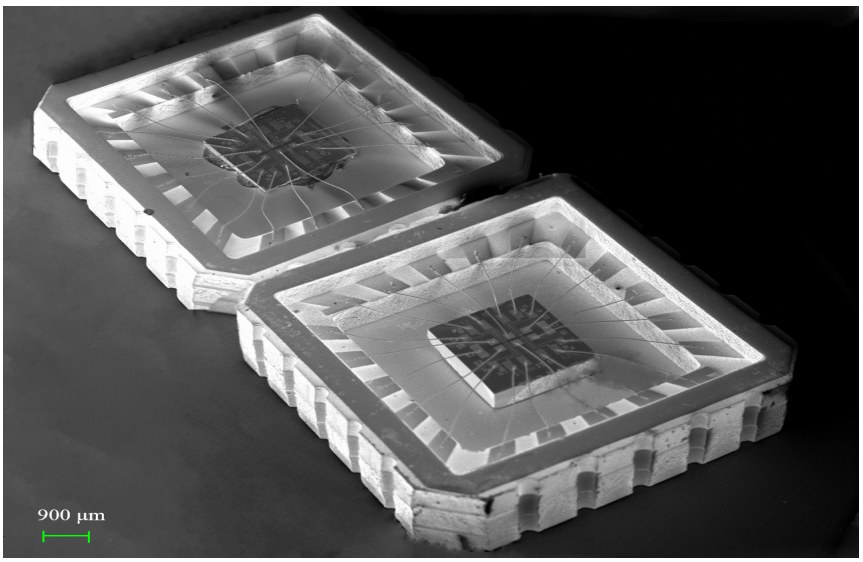

Figure 4.21: A scanning electron microscopy image of final fabricated chips packaged in LCCs for comparison, the top image is for packaged etched-chip with a back gate using conducting silver epoxy, and the bottom image is for un-etched chip without a back gate. In the latter case, non-conductive Ge-varnish was used to glue the chip to the base of LCC.

4.13 Packaging

Once the fabrication process is completed, the sample is then scribed and cleaved into individual chips. The chip is then cleaned in acetone and IPA before mounting on a 20 pin lead-less chip carrier (LCC). A ball of GE varnish or silver epoxy was placed in the middle of an LCC and the chip was mounted using toothpicks to hold them in position while the GE varnish or silver epoxy is left to be hardened for at least 10 minutes. Finally, the chips are bonded using a Au wedge bonder. A dummy device should always be used to find the optimum settings for bonding of Ohmic and gates contacts. The bonding pads of the gates might peel off if the power settings are too low. Figure 4.22 shows a fully packaged device where bonds are made to Ohmic contacts and gates using an Au wedge bonder.

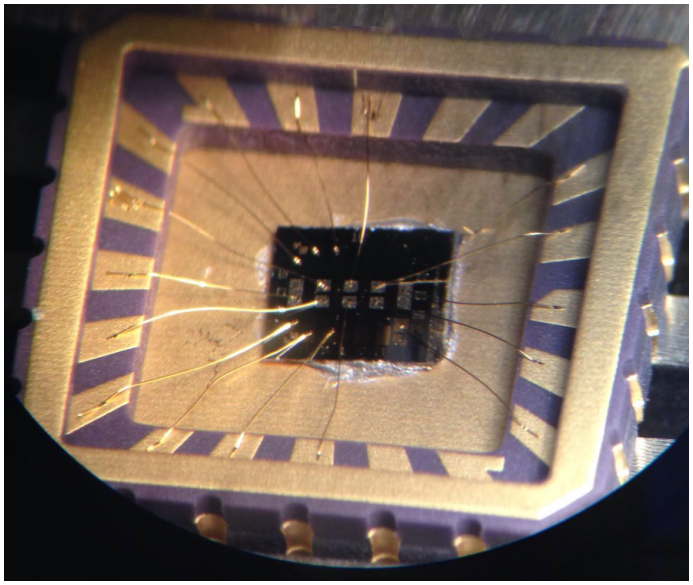

Figure 4.22: A microscopic image of a packaged device placed inside a 20 pin LCC using silver epoxy.

4.14 Summary

In this chapter, a detailed documentation of the fabrication process of making split-gates devices as well as the development of additional gates such as a mid-line gate, top gate and the back gate to make a systematic investigation of quasi-1D wires in the weak confinement regime.

Chapter 5

Wavefunction Mixing in laterally positioned One-dimensional wires

5.1 Introduction

The split-gate device on a GaAs/$Al_xGa_{1-x}As$ heterostructure was first demonstrated by Thornton *et al.* [14] in 1986 for the study of one-dimensional quantum interference and interaction effects. Since, the observation of the quantisation of conductance in ballistic 1D channels by Wharam *et al.* [15] and van Wees *et al.* [16], the split-gate device with the addition of extra gates have been used experimentally for investigating the transport of electron transport in one dimension.

The split-gate device offers confinement of the 2DEG to form a quasi-1D wire. The profile of the split-gate determines the potential seen by the electrons and also the electron density of the 2DEG. However, the standard split-gate device has limited control of the quantum wire. The development of additional gates like a mid-line, a top and a back gate offer independent control over the carrier density and the confinement potential [104–106]. This offers the flexibility in studying the regimes of low electron densities and weak confinement where electron-electron interactions can be seen [107].

This chapter presents the study of electron transport in weakly-confined quasi-

1D quantum wires for which the electron-electron interaction is supposed to be dominant. The experiments were performed using split-gate devices fabricated with an additional thin mid-line gate of 60 nm width, which allows relatively independent control over the confinement strength and the carrier density in the 1D wire. The width of the channel can also be varied using a magnetic field [108].

5.1.1 Horizontally-Aligned 1D Quantum Wires

There have been prior studies on interaction effects between horizontally aligned quantum wires. In 1989, Smith *et al.* managed to produce two parallel quantum wires in a single 2DEG using split-gate devices with a central dot gate [109]. The gates were swept simultaneously and the 1D subbands in the two channels were populated at the same rate as the result. The conductance trace had plateaus quantised in steps of $\frac{4e^2}{h}$ which is the sum of the conductance of two 1D wires.

In 1993, Simpson *et al.* measured a similar design to Smith's device which had independent control of the two arms of the split-gate and the dot gate. This gives the flexibility to adjust independently the widths of the channel and the size of the dot. When both channels were populated symmetrically, quantisation was observed in steps of $\frac{4e^2}{h}$ [3]. Figure 5.1 shows the study performed by Simpson *et al.* where one arm of the split-gate was kept at a fixed voltage, the opposite arm of the split-gate was incremented in steps of 5 mV, and at each value the dot voltage was swept from 0 V to the point where both constrictions were pinched off. As a result, the number of subbands in each channel was varied simultaneously and when both channels depopulated symmetrically, the quantisation was observed in steps of $\frac{4e^2}{h}$.

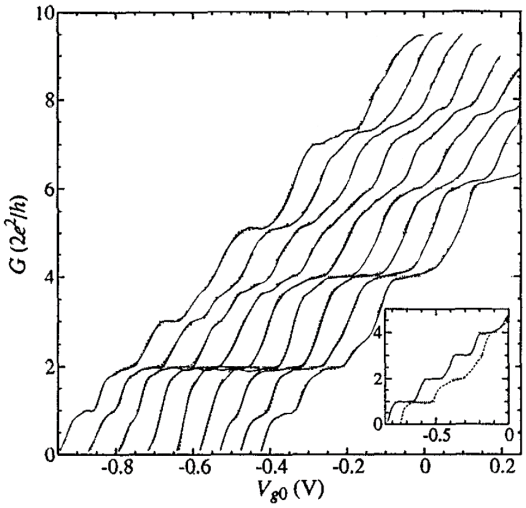

Figure 5.1: Solid curves: The conductance characteristics with both constrictions open, one arm of the split-gate is held at -1.1 V and the other is incremented from -1.55 to -2.35 V in 10 mV steps. Each curve is offset by 10 mV for clarity. The lower inset shows the two single channel characteristics summed to obtain the left-hand curve. Graph is adapted from Ref [3].

In 1991, Hwang *et al.* had managed to produce two independently tunable quantum wires horizontally by etching a dot in the centre of the constriction of a split-gate device with a diameter of 200 nm. The number of subbands occupied in the QPC on either side of the dot can be tuned independently by the gate, with each channel having conductance steps in units of $\frac{2e^2}{h}$ to produce quantisation steps of $\frac{4e^2}{h}$ [110].

5.1.2 Vertically-Aligned 1D Quantum Wires

The MBE growth technique has allowed very precise control of wafers growth which allows the creation of a double quantum well with an $Al_xGa_{1-x}As$ barrier the width of which can be tuned. This allowed the possibility for two parallel

and closely separated quasi-1D channels which gives rise to interactions between the wires.

Previous work was done where a mid-line gate with split-gate devices were fabricated on GaAs/$Al_xGa_{1-x}As$ double quantum well heterostructures and measurements were performed to study the effects of the interaction between two parallel wires [4, 111–114]. Both split-gate define a 1D channel in both 2DEGs simultaneously and the mid-line gate controls the density in one of the 1D wires.

Castleton *et al.* measured GaAs/$Al_xGa_{1-x}As$ double quantum wells with 30 nm and 2.5 nm $Al_xGa_{1-x}As$ barriers, respectively [4]. There are two regions when both wires behaved independently, and a region when both wires were populated simultaneously. Figure 5.2 (a) shows G_{12} for a device with split-gate and a mid-line gate in-between with a 30 nm $Al_xGa_{1-x}As$ barrier as a function of V_{sg} for increments of V_{mg} from 0.50 V to -0.48 V in 20 mV increments. Three regions are observed in the graph. Firstly, the triangular areas at the bottom right and bottom left 'U' and 'L' arise from a single quasi-1D wire in either layers of the 2DEG where both wires had conductance plateaus in steps of $\frac{2e^2}{h}$. In the middle region, two 1D wires are conducting in parallel with a conductance equal to the sum of both wires which is characteristics for uncoupled wires. Figure 5.2 (b) shows the transconductance plot, $\frac{\delta G_{12}}{\delta V_{sg}}$, of data from (a), as a function of V_{mg} and V_{sg}. Areas U and L show the subbands of a single 1D wire in either 2DEG. There is a region of double-wire mixing together giving rise to bonding and anti-bonding states.

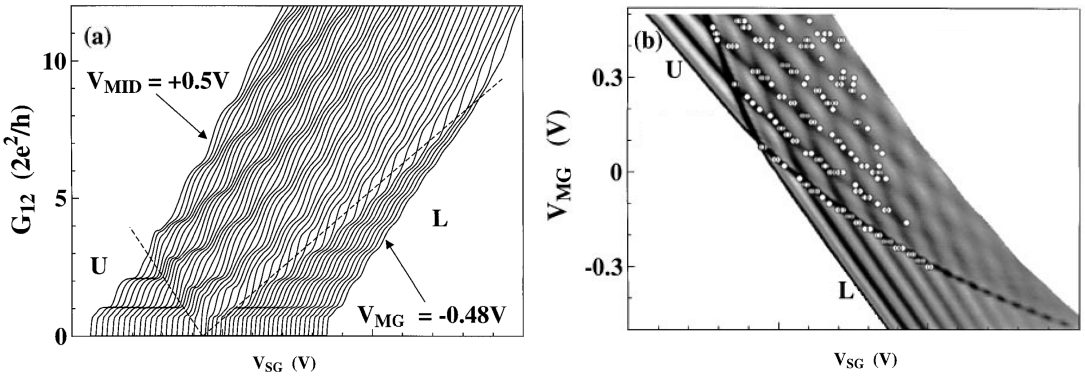

Figure 5.2: (a): Conductance traces of a double-quantum-wire device with a 30 nm $Al_xGa_{1-x}As$ barrier. V_{sg} is swept for fixed V_{mg}, where V_{mg} is incremented between traces from 0.5 V to -0.48 V. A single wire conducts in regions of U and L delineated by a dashed line from the region in which both wires conduct in parallel (b): transconductance plot, $\frac{\delta G_{12}}{\delta V_{sg}}$, of data from (a), as a function of V_{mg} and V_{sg}. Light regions indicate ballistic plateaus and dark regions indicate risers between plateaus . Both (a) and (b) are adapted from Ref [4].

5.1.3 Motivation

The coupling between the two 1D wires depends on the interaction and overlap between their wavefunctions. Thomas and Castleton *et al.* [112, 113] measured two quantum wires with a separation between the double quantum wells around 30 nm. Previously, double quantum well wafers were favoured as it can produce 1D wires that can be much closer together than laterally patterned parallel 1D wires formed in a single 2DEG [3, 109, 110]. It is challenging to create two 1D wires closely separated in a single 2DEG by electrostatic gating due to limitations in lithographic resolution [4]. In the present work, split-gate devices with mid-line gates were fabricated and the mid-line gates were carefully patterned with width varying from 20 to 80 nm in an attempt to create two 1D wires closely separated in a single 2DEG.

5.1.4 Device Design

A mid-line gate is deposited on the surface of GaAs/$Al_xGa_{1-x}As$ heterostructure in between the split-gate. By applying either a negative or positive voltage to the mid-line gate, electrons are either repelled or attracted from the 2DEG. Thus, the mid-line gate can control the electron density in the 1D wire. A strong negative bias on the mid-line gate could divide the channel into two laterally 1D wires and if the width of the mid-line gate is thin, it may allow interactions between the two 1D wires. A 300 nm cross-linked PMMA layer was deposited on the channel below the metal track connecting the mid-line and the optical gate to reduce any asymmetry effects in the channel arising from the track and therefore, only allowing the mid-line gate to be on the surface of the channel. The disadvantages of this design is the additional two electron beam lithography stages, first is exposure of the cross-linked dielectric layer and the second is the deposition of the mid-line gate itself. Figure 6.2 shows a schematic of the mid-line gate in between the split-gate with cross-linked PMMA deposited underneath the tracks connecting the mid-line gates.

5.1.5 Measurement

Split-gate devices with a thin mid-line gate used in the present work were fabricated on a delta doped GaAs/$Al_xGa_{1-x}As$ heterostructure. The two-dimensional electron gas is located 286 nm below the surface, with electron density, n_{2d} $2.2 \times 10^{11} cm^{-2}$ and mobility μ of $7.95 \times 10^6 cm^2/Vs$; further details of the wafer used, W731, is given in appendix A. The split-gate devices has a length of 400 nm and width of 700 nm and the mid-line gate has a width of 60 nm. The

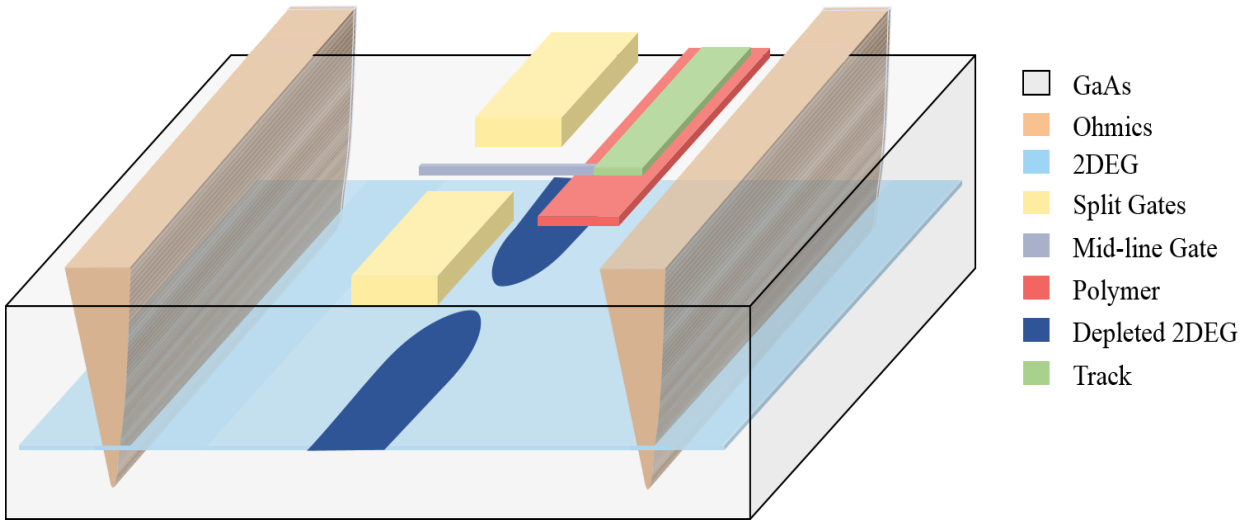

Figure 5.3: A schematic diagram of a mid-line-gated with split-gate device.

measurements were performed in a cryogen-free dilution refrigerator with a base temperature of 10 mK and electron temperature of 70 mK. Two terminal differential conductance $G = \frac{dI}{dV}$ was measured with a sinusoidal excitation voltage of 10 μV at frequency of 77 Hz. The magnetic-field measurements were conducted with the field perpendicular to the plane of the 2DEG.

5.1.6 Mode of Operation

The split-gate devices with a mid-line gate devices are operated by applying a fixed voltage on the mid-line gate, V_{mg}, and sweeping the negative voltage applied to the split-gate, V_{sg}. The voltage applied to the split-gate creates the 1D wire and controls mainly the strength of the confining potential in the transverse direction. The mid-line gate controls the density in the 1D wire and can be varied using, V_{mg}.

Figure 5.4 shows the conductance plot of a split-gate device with a standard

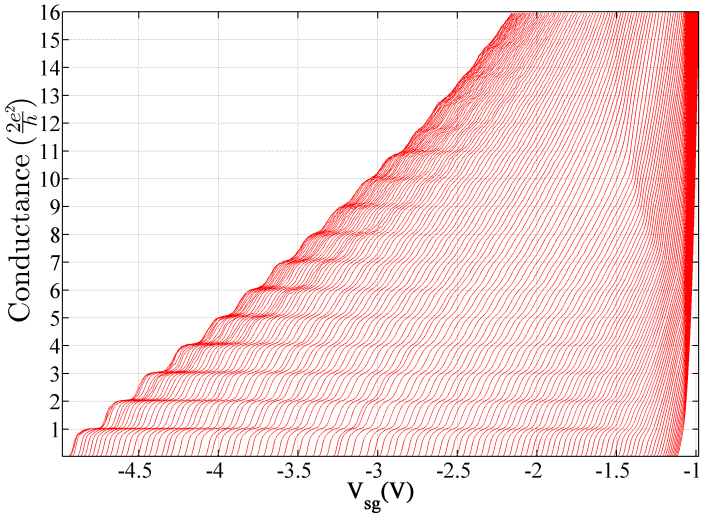

Figure 5.4: Conductance data from a mid-line gated device at T = 10 mK and electron temperature of $\sim$ 70 mK. For each trace V_{sg} is swept and V_{mg} is fixed. V_{mg} is incremented in steps -30 mV intervals from 0.1 V on the left to -5.0 V on the right. The split-gate have dimensions of 400 nm in length and 700 nm in width, with a 80 nm wide mid-line gate.

mid-line gate of a width of 80 nm. For each trace, the conductance is measured as a function of V_{sg} at a fixed value of mid-line gate, V_{mg}. V_{mg} is incremented in steps of 30 mV intervals from 0.1 V on the left to -5.0 V on the right. As V_{mg} becomes more negative, the electrostatic potential confining the 1D channel becomes stronger. The conductance traces from left to right means that 1D wire is moving from a stronger confined regime to a weakly confined regime. The plateaus become shorter and less defined as the device move from strong to weak confinement. The mid-line, V_{mg}, controls the density of the electrons in the channel between the split-gate. As V_{mg} becomes more negative, the pinch-off voltage of V_{sg} moves to less negative voltages which is consistent with a lower carrier density [104].

Figure 5.5 shows the greyscale plot of data, shown in figure 5.4. When no

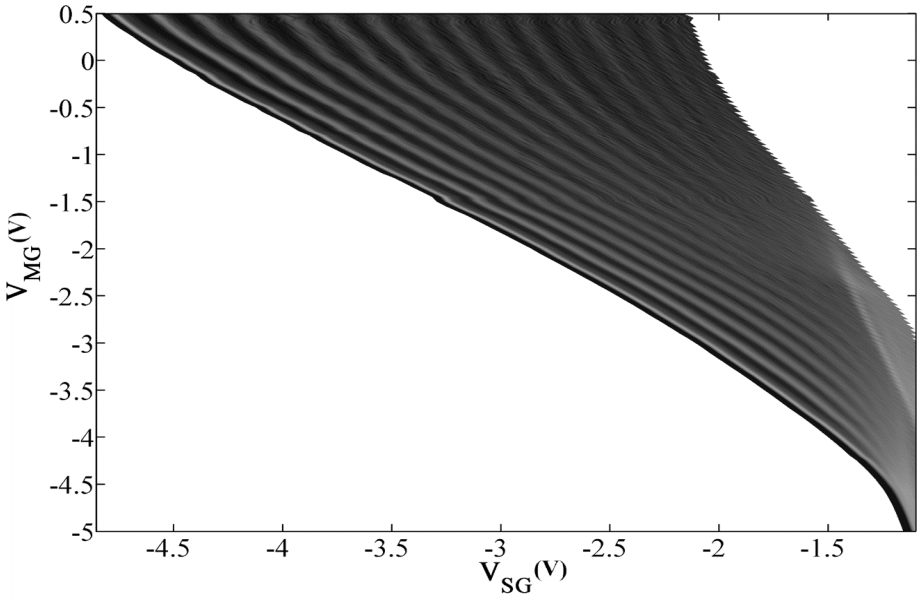

Figure 5.5: Greyscale plot of transconductance of the data in figure 5.4, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

voltage is applied on the mid-line gate, the 1D system is in the strong confinement regime, on making the mid-line gate progressively negative this results in weakening the confinement eventually all the plateaus smear out at $V_{mg} \sim$ -4 V (figure 5.5).

5.2 Results

The section shows the conductance results on a mid-line gated split-gate device with mid-line gate width of 60 nm. One of the major results in this chapter is the possible formation of two horizontally aligned 1D wires in a single 2DEG.

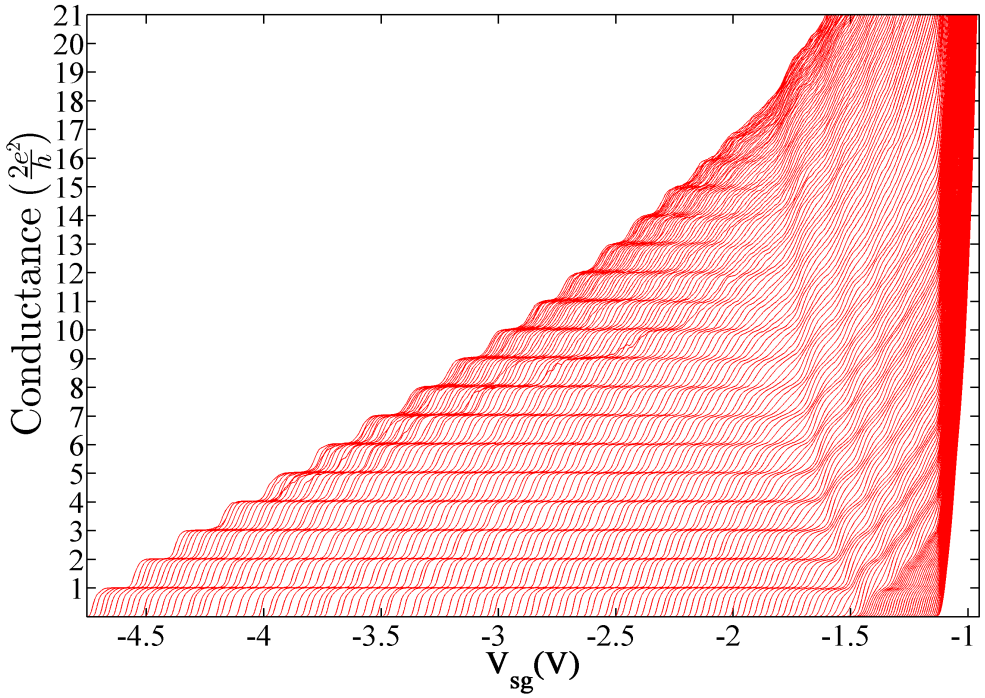

Figure 5.6: Conductance data from a mid-line gated device at T = 10 mK and electron temperature of $\sim$ 70 mK. For each trace V_{sg} is swept and V_{mg} is fixed. V_{sg} is incremented in steps -30 mV intervals from 0.0 V on the left to -5.9 V on the right. The split-gate have dimensions of 400 nm in length and 700 nm in width, with a 60 nm wide mid-line gate.

Figure 5.6 shows three distinct regions are observed. The regions at the right side and bottom left arise from a single quasi-1D channel on either side of the mid-line gate. Both 1D wires exhibit quantised ballistic conductance plateau in steps of $\frac{2e^2}{h}$. In the mixed region, two 1D wires are present and conduct in parallel with a total conductance equal to the sum of the conductance of each wire in steps of $\frac{4e^2}{h}$. There is a smooth transition of conduction from one wire to other while maintaining the ballistic conductance. Comparing the effect of the mid-line gate on the conductance behaviour in figures 5.4 and 5.6, it can be seen that a wide mid-line gate of 80 nm tunes the density of the channel while a 60 nm

thin mid-line gate is capable dividing the channel to create two 1D wires. Figure 5.7 shows a blow up of figure 5.6 at the transition where two 1D wires conduct simultaneously in steps of $\frac{4e^2}{h}$.

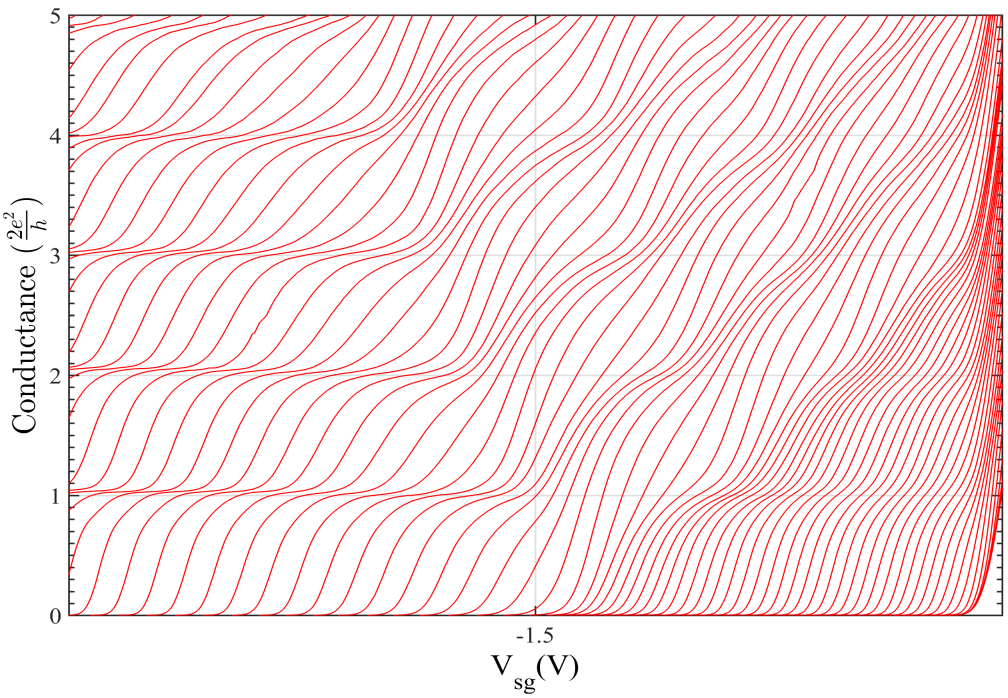

Figure 5.7: A blow up of conductance data of figure 5.6 at the transition where two 1D wires conduct simultaneously. For each trace V_{sg} is swept and V_{mg} is fixed. V_{sg} is incremented in steps -30 mV intervals. The split-gate have dimensions of 400 nm in length and 700 nm in width, with a 60 nm wide mid-line gate.

To understand the conductance characteristics better, figure 5.6 is differentiated with respect to V_{sg} to produce the grey scale plot shown in figure 5.8. The black lines correspond the transconductance $\frac{dG}{dV_{sg}}$ maxima between plateaus, indicating where a 1D sub-band edge crosses through the chemical potential. The 1D sub-band edges are therefore represented by the red lines in figure 5.10. A mixing region is depicted by the two sets of lines overlapping where crossing of

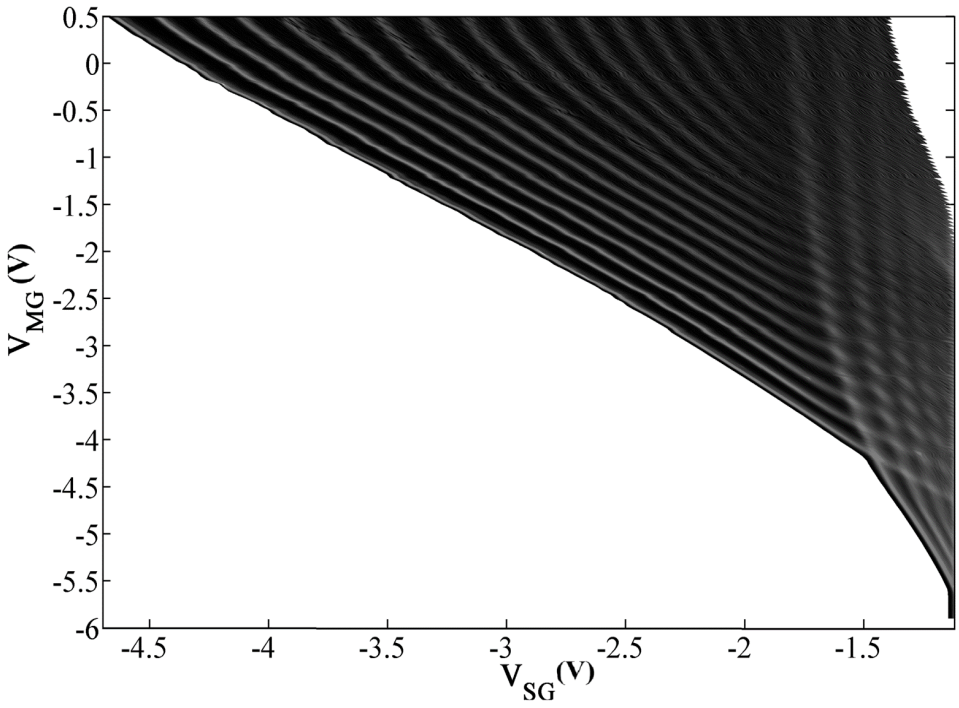

Figure 5.8: Greyscale plot of transconductance of the data in figure 5.6, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

1D subbands from each wire is shown clearly in figure 5.8 which indicates that subbands of each wire are populated simultaneously. Figure 5.9 shows a blow up of figure 5.8 at the transition where two 1D wires conduct simultaneously in steps of $\frac{4e^2}{h}$.

Figure 5.10 shows solid lines representing the maxima of $\frac{dG}{dV_{sg}}$ which corresponds to subbands of the 1D wires. The red solid lines correspond to subbands from the first 1D wire while the blue solid lines correspond to subbands from the other 1D wire. The crossing of the 1D subbands between the two wires are smooth and that the two wires are clearly uncoupled [5, 115]. Castleton *et al.* performed

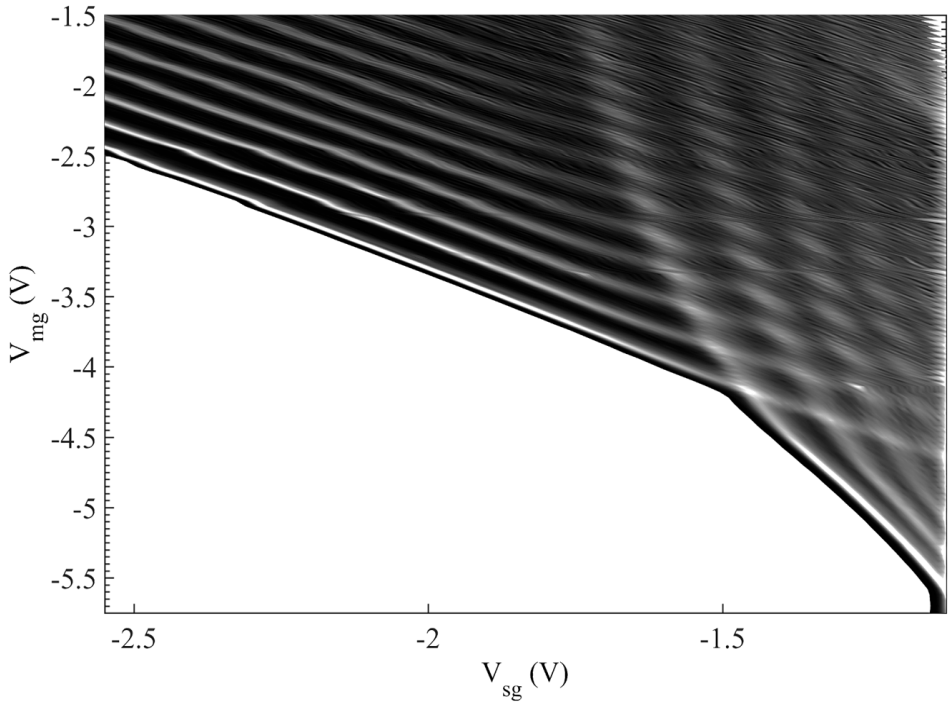

Figure 5.9: A blow up of the greyscale plot in figure 5.8, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg} at the transition where two 1D wires conduct simultaneously in steps of $\frac{4e^2}{h}$. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

similar measurements of two uncoupled 1D wire using devices fabricated on a DQW wafer which contained two 15 nm wide quantum wells separated by a 30 nm $Al_xGa_{1-x}As$ barrier [4]. In addition, Thomas and Castleton *et al.* measured mid-line gated devices on a DQW where the $Al_xGa_{1-x}As$ barrier was 30 nm and in these devices the 1D wires in each well were un-coupled, and showed that the 1D sub-bands in the both wires simply add up [4, 112].

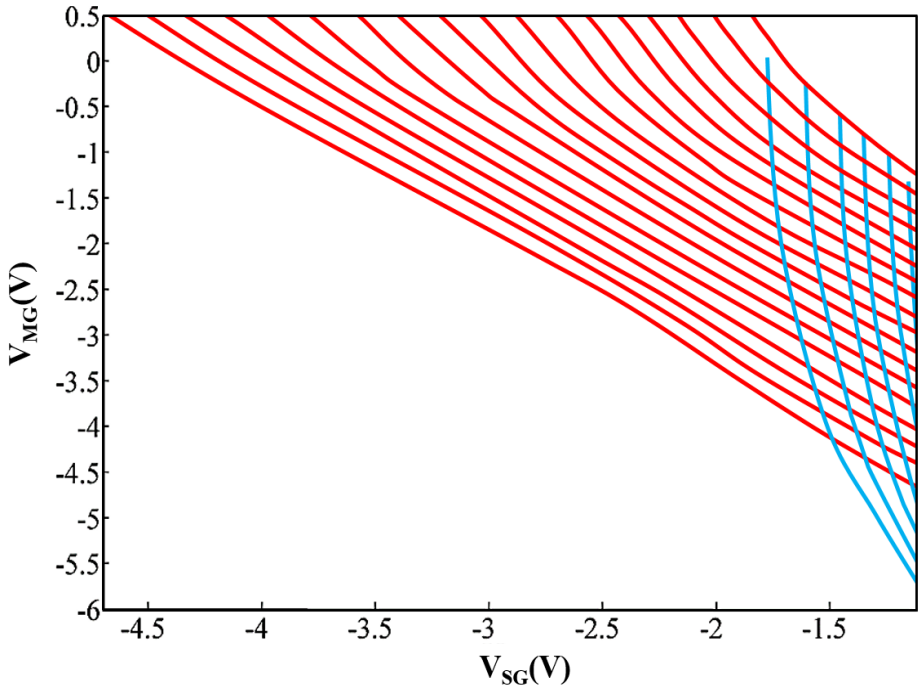

Figure 5.10: Solid lines represent the maxima in $\frac{dG}{dV_{sg}}$ of the data presented in figure 5.6. The red solid lines correspond to subbands from the first 1D wire while the blue lines correspond to subbands from the second wire.

5.2.1 Perpendicular Magnetic field

The section describes the effect of applying a perpendicular magnetic field on the conductance traces. It is shown that the application of a perpendicular magnetic field widens the sub-band spacing of the 1D wire compared to no magnetic field [116]. The application of perpendicular magnetic field changes the conductance plateaus as they increase in length, across the whole range of confinement. This reflects an increased subband spacing due to the additional confinement from the magnetic field and subsequent magnetic depopulation of higher 1D subbands. The conductance and the quality of the quantisation should improve and be cleaner in

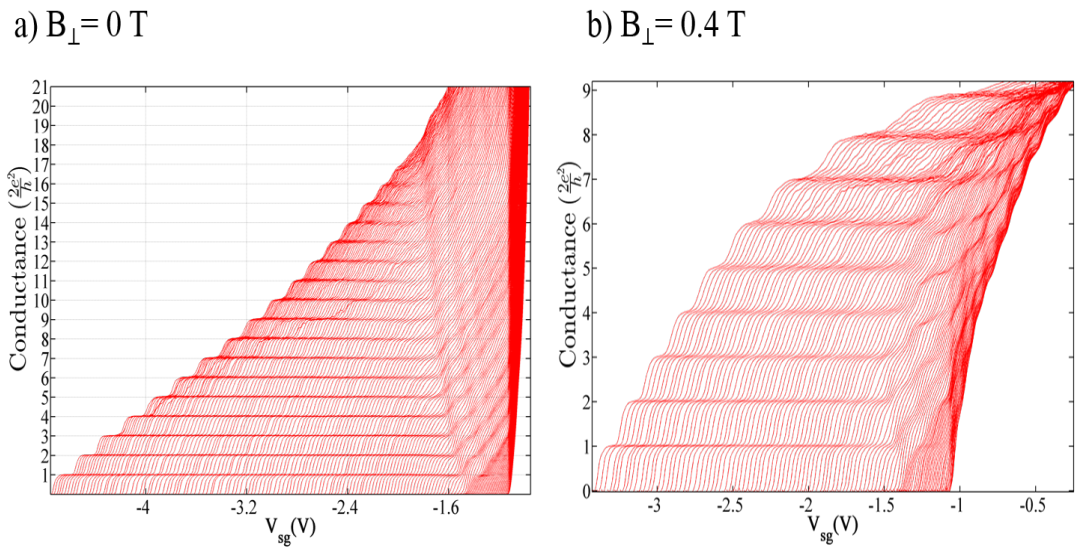

Figure 5.11: Conductance data from a mid-line gated device at T = 10 mK and electron temperature of $\sim$ 70 mK. For each trace V_{sg} is swept and V_{mg} is fixed. V_{mg} is incremented in steps -30 mV intervals from 0.1 V on the left to -5.0 V on the right. A perpendicular magnetic field has been applied a) 0.0 T b) 0.4 T.

the presence of a perpendicular magnetic due to the reduction of backscattering [116, 117]. Figure 5.11 (b) shows the conductance plot in presence of a perpendicular field of 0.4 T where the region of plateaus in the first wire increase in length which reflects an increased subband spacing and also magnetic depopulation of higher subbands compared to that of 0 T in figure 5.11 (a). In addition, the region of double-wire mixing together has been reduced by the perpendicular magnetic field. This magnetic-field behaviour shows there is no existence of an impurity in or near the 1D wire.

Figure 5.12 shows the greyscale plot of the device measured in different perpendicular magnetic fields varied from 0.0 T to 0.6 T in steps of 0.1 T. The regions at the right side shows the subbands arising from a single quasi-1D channel and the regions at the left side shows the subbands arising from the other

single quasi-1D channel which shows three subbands. As the magnetic field is increased, the subband spacing increases and magneto-electric depopulation of higher subbands occurs where subbands depopulates from twenty subbands at zero field to six subbands at 0.6 T. The mixing region where both subbands of the wires add up decreases when the perpendicular magnetic field increased. At 0.6 T, the mixing region has decreased to just the mixing of the first subbands. The mixing regime disappears with increasing magnetic field due to increase in the lateral separation of the edge states in the different 1D wire. The application of a perpendicular magnetic field localise the wavefunction of electrons thus reducing the overlapping of two 1D wires. Figure 5.12 (f) shows only a few Landau subbands which exhibit a large level of repulsion in the order of $\hbar\omega_c$.

5.2.2 Lateral Shifting of 1D Wire

Asymmetric voltage bias can be applied to the arms of the split-gate to laterally shift the 1D wire [118, 119]. It is used to move the 1D wire across the channel to probe the variation of potential in the channel or to move the 1D wire away from an impurity. In this section, the conductance is measured by changing the offset voltages on the arm of the split-gate by applying an offset voltage on one gate and sweep both split-gate together. Williamson *et al.* estimated the distance of the shift of the 1D wire across the channel and is given as [120]

$$x_{min} = \left(\frac{l}{2}\right)\frac{V_1 - V_2}{V_1 + V_2} \tag{5.1}$$

where x_{min} is the position of the potential minimum of the 1D channel, l is

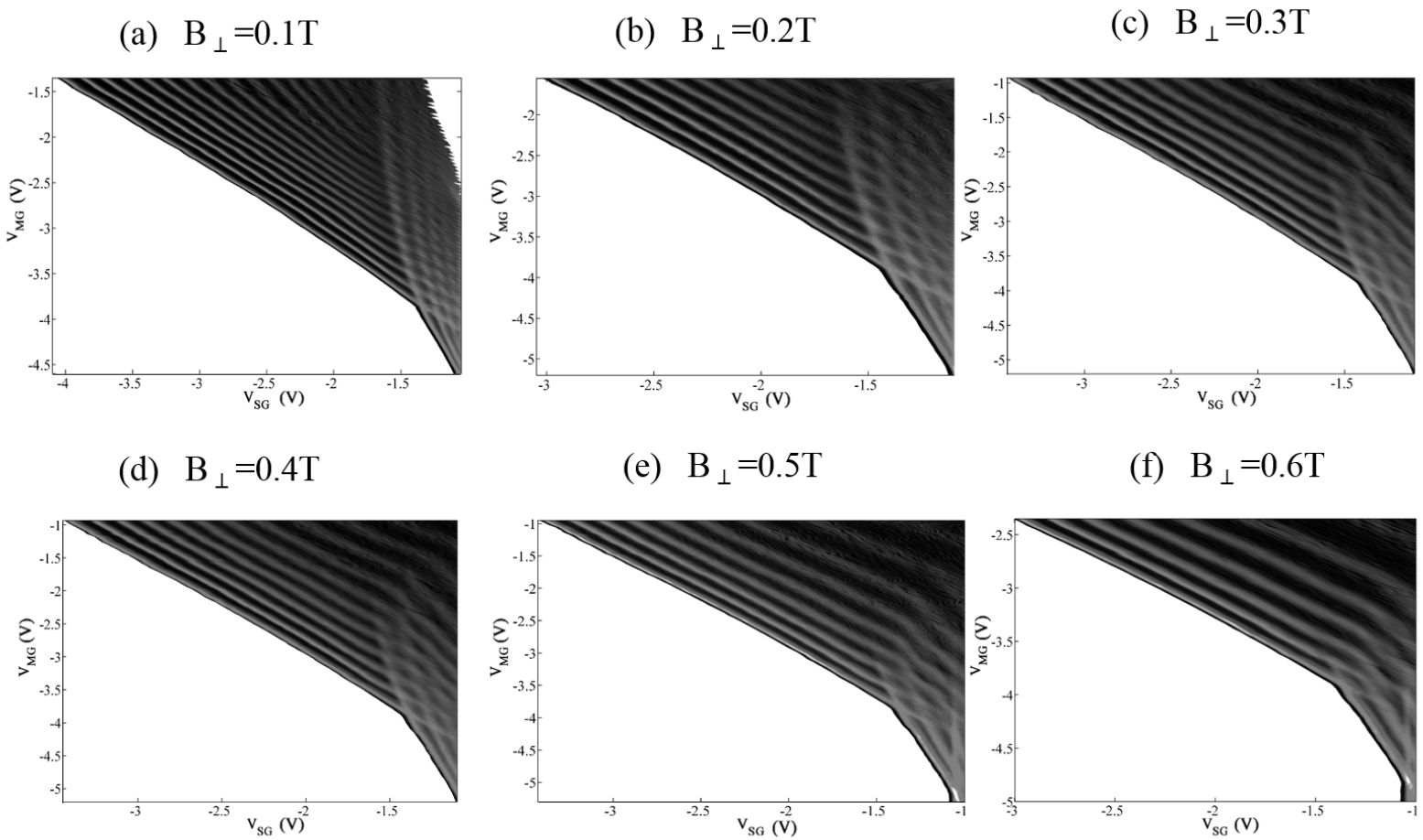

Figure 5.12: Greyscale plot of transconductance of the data in figure 5.6, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

the split-gate separation, and V_1 and V_2 are the voltages applied to the right and left arms of the split-gate, respectively. If the asymmetric bias is large enough, the channel can moved far away from any impurity existing in the channel.

5.2.2.1 Laterally shifting the 1D Channel

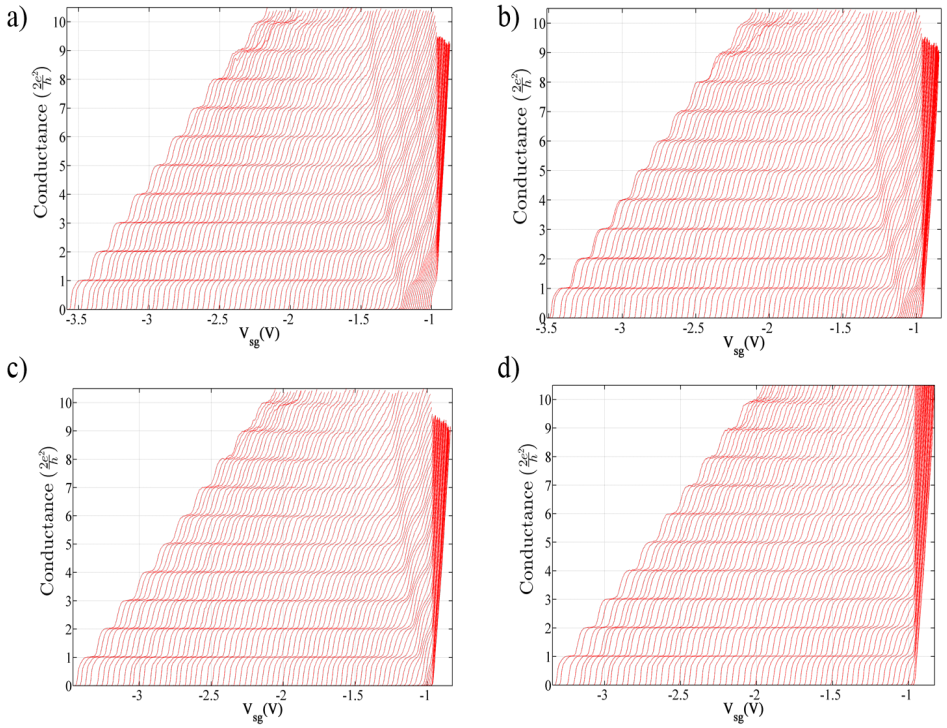

Figure 5.13: Conductance characteristics of the sample as the 1D channel is shifted laterally. The conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -30 mV in all the plots. In a) the 1D channel is laterally shifted by applying an offset of 0.1 V between the arms of the split-gate. In b) the channel is shifted with an offset of 0.2 V. In c) the channel is shifted with an offset of 0.3 V. In d) the offset is increased to 0.5 V.

Figures 5.13 (a) to (d) show the conductance characteristics of the sample for different bias voltages between the two arms of the split-gate. Figure 5.6 shows

a symmetric bias is applied and V_{mg} is stepped from 0.0 V on the left to -5.9 V on the right in intervals of -30 mV. In figure 5.13 (a) an offset of 0.1 V is applied, which laterally shifts the 1D channel in one direction. In figure 5.13 (b) the channel is shifted by 0.2 V. The channel is shifted further in the same direction in figure 5.13 (c) and (d) where an offset of 0.3 and 0.5 V is applied respectively. It is important to note that the plateaus are well defined and do not change in length which reflects no change in the subband spacing due to the asymmetric bias. As the left arm is incremented by a positive offset, V_2, by 0.1 V, the higher plateau of the right-side 1D quantum wire disappear, leaving only two plateaus in the 1D wire and the mixing regime has also decreased. The arm of the split-gate is incremented further by a positive offset, V_2, of 0.2 V, resulting in the second plateau disappearing in the right-side 1D quantum wire, leaving only one plateau in the 1D wire which results in the mixing regime reducing further. The arm of the split-gate is incremented further by a positive offset, V_2, of 0.5 V, resulting in all the quantised plateaus of the right-side 1D wire disappearing, leaving only left-side 1D wire conducting which results in the disappearance of the mixing regime as well.

Figure 5.14 shows a more detailed picture in the greyscale plot of data shown in figure 5.13 where a positive asymmetric voltage is applied on the left arm of the split-gate, V_2, from 0.1 V to 0.5 V in steps of 0.1 V. The higher subbands of the right-side 1D wire starts disappearing gradually as the asymmetric voltage, V_2, is increased and the 1D wire disappears completely by applying an offset of 0.5 V and only the subbands of the first wire are visible. Using equation 5.1, the 1D wire was estimated to shift in the strong-confinement regime: V_1=-1.49 V and V_2=-0.99 V, giving x_{min} = 84.5 nm. A lateral shift of 1D wire by 84.5 nm is

needed to remove the second 1D wire and its mixing region. This confirms that the creation of the two wires is by means of electrostatic effects only and not by an impurity sitting in the 1D channel.

To examine the symmetry in the channel, the conduction channel was laterally shifted by applying an asymmetric voltage on the other arm of the split-gate, V_1. A negative voltage was applied to the right arm of split-gate. Figure 5.15 shows the greyscale plot of where a negative asymmetric voltage is applied on the right arm of the split-gate, V_1, from -0.1 V to -0.5 V in steps of -0.1 V. Similar to figure 5.14, the higher subbands of the right-side 1D wire starts disappearing gradually as the asymmetric voltage, V_1, is increased and the 1D wire disappears completely by applying an offset of -0.5 V and only the subbands of the first wire are visible. This confirms that the potential in the channel is symmetric.

5.2.2.2 Laterally shifting the 1D Channel in Reverse Direction

The 1D channel was laterally shifted in the opposite direction by applying a positive asymmetric voltage on the other arm of the split-gate, V_1. Figures 5.16 (a) to (d) show the conductance characteristics of the sample for different positive asymmetric voltages applied on right-side arm of the split-gate, V_1. Figure 5.16 (a) shows a symmetric bias is applied and V_{mg} is stepped from 0.0 V on the left to -5.9 V on the right in intervals of -30 mV. In figure 5.16 (b) an offset of 3.5 V is applied, which laterally shifts the 1D channel in the other direction. In (c) the channel is shifted by 6.5 V. The channel is shifted further in the same direction (d) where an offset of 7.7 V is applied respectively. It is important to note that the plateaus are well defined and do not change in length which reflects no change in the subband spacing due to the asymmetric bias. As the

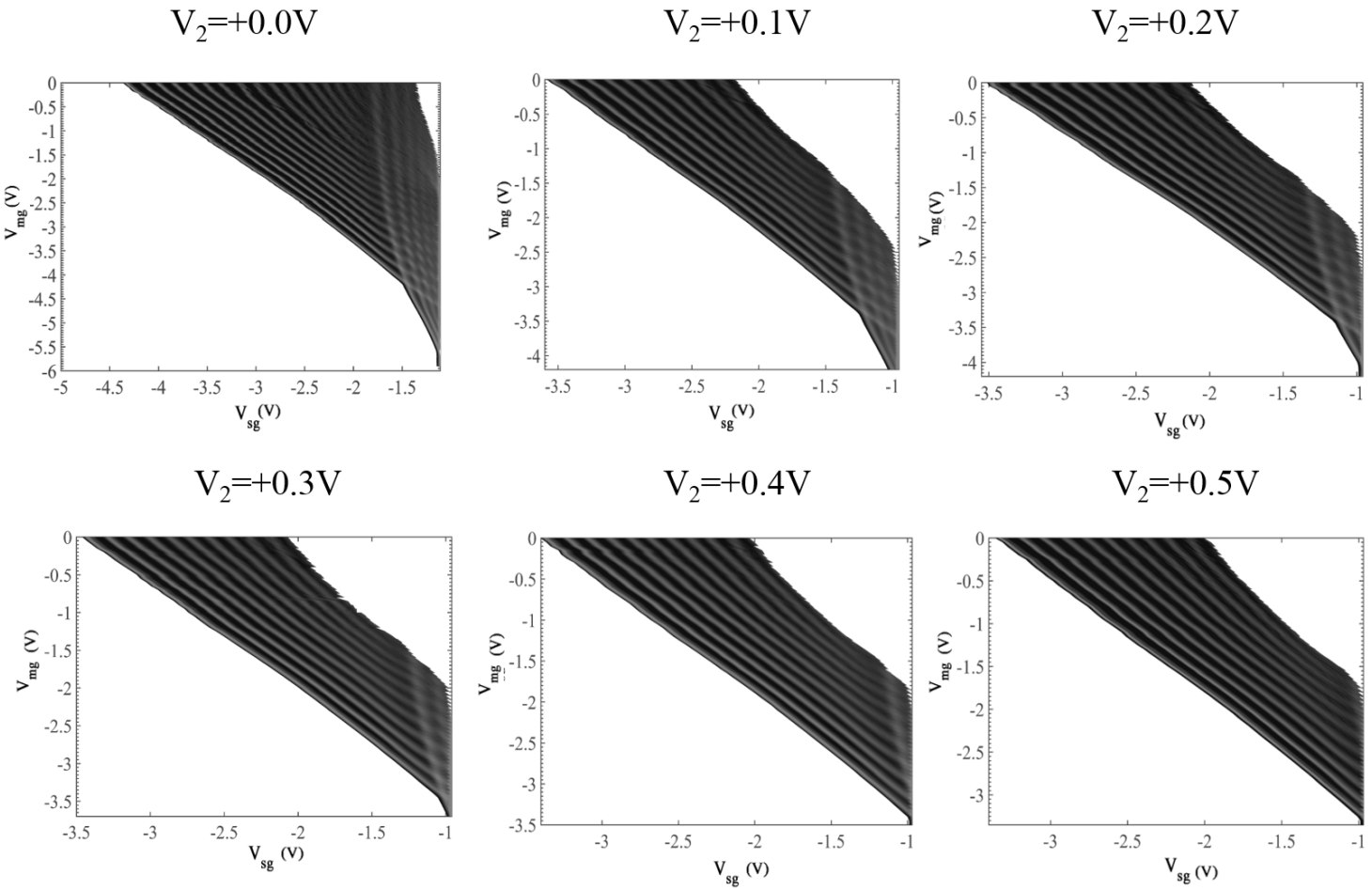

Figure 5.14: Greyscale plot of transconductance of the data in figure 5.6, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

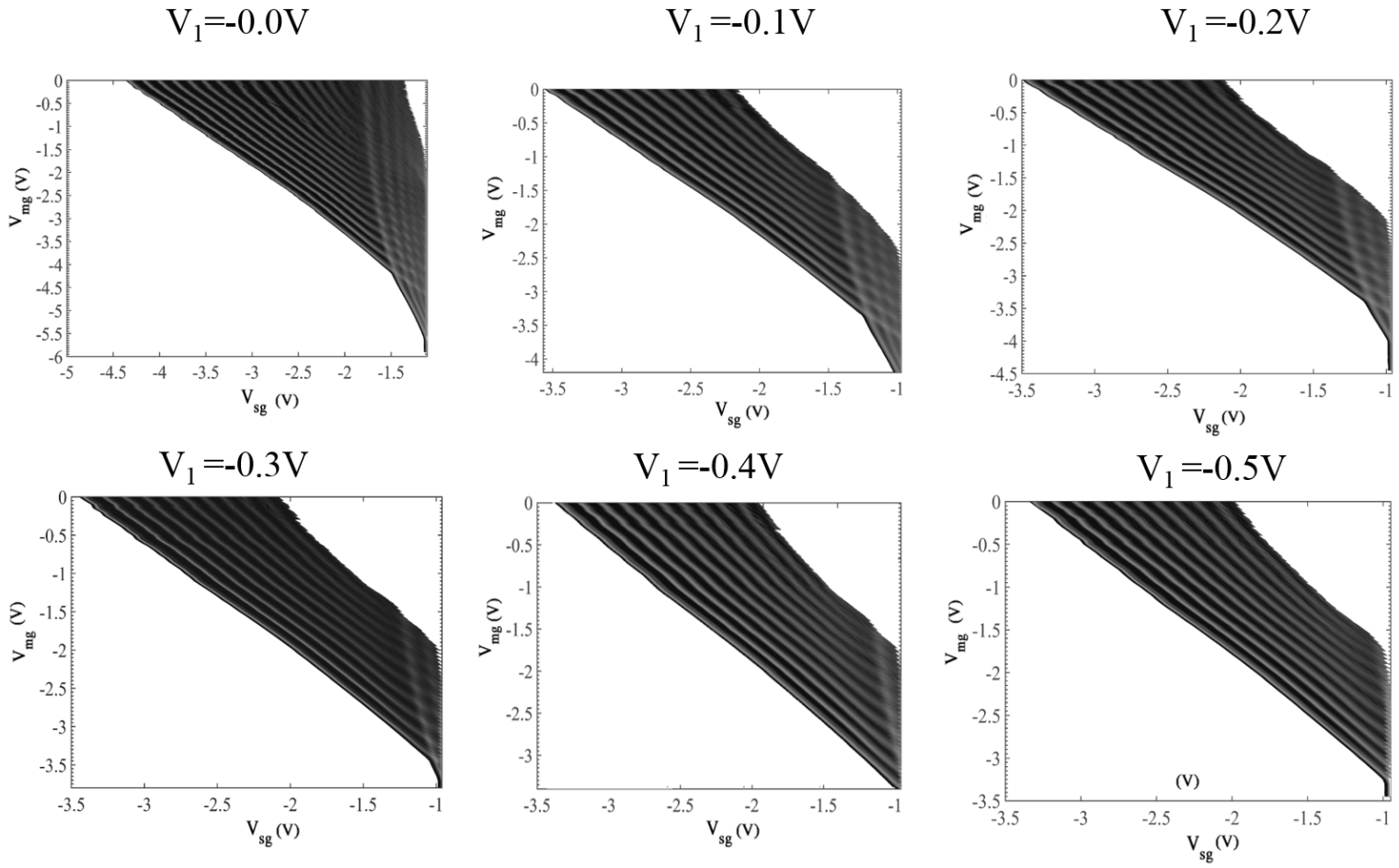

Figure 5.15: Greyscale plot of transconductance of the data in figure 5.6, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

arm is incremented by a positive offset, V_1, the higher plateaus of the left-side 1D quantum wire disappear, leaving only five plateaus in the 1D wire and the mixing regime has also decreased. The arm of the split-gate is incremented further by a positive offset, V_1, of 6.5 V, resulting in the left-side 1D wire disappearing leaving only a reduced mixing regime. The arm of the split-gate is incremented further by a positive offset, V_1, of 7.7 V, resulting in all the quantised plateaus disappearing from the left-side 1D quantum wire, leaving only the right-side 1D wire conducting and the mixing regime has also disappeared. Using equation 5.1, the 1D wire was estimated to shift in the week-confinement regime: V_1=-1.07 V and V_2=-8.77 V, giving x_{min} = 274.0 nm. A lateral shift of 1D channel by 274.0 nm is needed to remove the first 1D wire and its mixing region. This confirms that the creation of the two wires is not made in the middle of the channel. Figure 5.17 shows the greyscale plot of where a positive asymmetric voltage is applied on the right arm of the split-gate, V_1, from 3.5 V to 7.7 V. The higher subbands of the left-side 1D wire starts disappearing gradually as the positive asymmetric voltage, V_1, is increased and the 1D wire disappears completely by applying an offset of 7.7 V and only the subbands of the other, smaller 1D wire are visible.

5.2.3 Sub-band Spectroscopy Measurements

The energy subbands of a 1D wire can be examined using a finite bias across the quantum wire. Patel *et al.* had developed the measurement technique to measure the subband energy of 1D wires after it was theoretically predicted by Glazman [50, 52, 53, 121]. The differential conductance $G = dI/dV_{sd}$ with a finite dc source-drain bias voltage, V_{sd}, is measured by using a lock-in technique

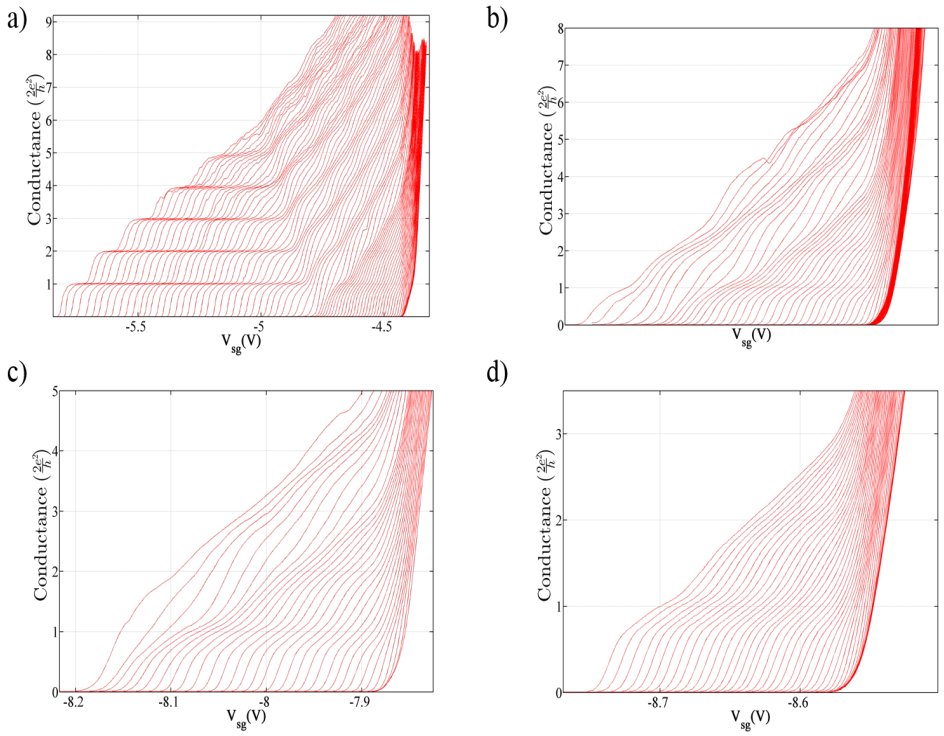

Figure 5.16: Conductance characteristics of the sample as the 1D channel is shifted laterally. The conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -30 mV in all the plots. In a) the 1D channel is laterally shifted by applying an offset of 3.5 V between the arms of the split-gate. In b) the channel is shifted with an offset of 6.5 V. In c) the channel is shifted with an offset of 7.0 V. In d) the offset is increased to 7.7 V.

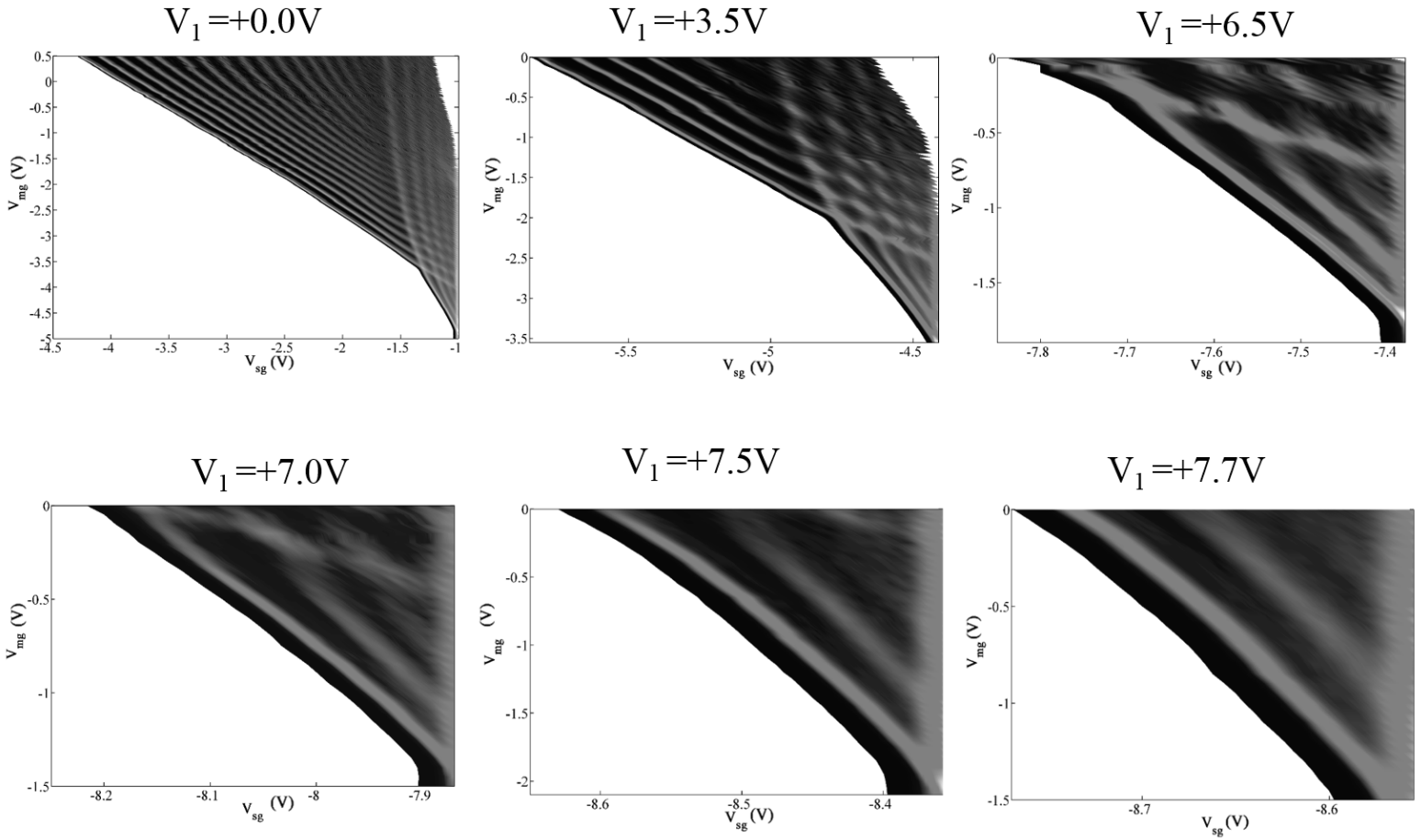

Figure 5.17: Greyscale plot of transconductance of the data in figure 5.6, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

where an ac signal is superposed with a dc source-drain bias voltage was applied. Sub-band spectroscopy measurements were performed along the spectrum of 1D regime from strong confinement to the weak confinement. Figure 5.18 shows the traces selected for dc bias measurement in the regions of left-side 1D wire, the mixing regime and right-side 1D wire by varying the mid-line gate voltages.

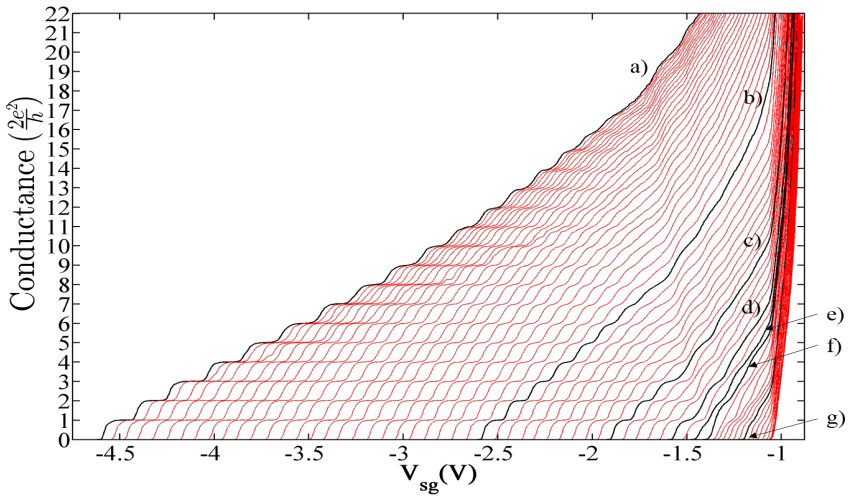

Figure 5.18: Conductance characteristics of the 1D channel and the conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -50 mV in all the plots. The bold, black traces from left to right correspond to sub-band spectroscopy performed in different regions of 1D wire where different mid-line gate voltages, V_{mg}, have been applied a) to g).

Figure 5.19 shows the greyscale of the dc-bias measurements of traces (a) to (d) shown in figure 5.18 where the dc bias voltage of 3 mV to -3 mV in steps of 0.1 mV is applied between source and drain of the device. Diagonal branches that cross are observed in the greyscale plots and a branch that moves upwards as the magnitude of the source-drain bias increase indicates that the chemical potential at the drain falling through the bottom of a sub-band and the downward

moving branch indicates that the source chemical potential is rising through the bottom of a sub-band. When the sub-bands cross, the source and drain chemical potentials are passing through sub-band minimum simultaneously. The crossing of the sub-bands at a non-zero source-drain bias corresponds to the source and drain potentials being at the bottom of adjacent sub-bands and the sub-band energy spacing can be deduced from it. The transconductance maximum in grey shows the coincidences of the chemical potential of the source or drain reservoir with 1D subband edges. The energy separation between subsequent 1D-subband edges can be deduced from the diamond patterns of the transconductance maxima (grey colour) on the drain bias voltage scale and is given by equation [53, 122]

$$\Delta E_{(n,n+1)} = \frac{e}{2}(V_1 + V_2) \tag{5.2}$$

where E is subband spacing and V_1 is the source-drain voltage at which the first extremum in d^2I/d^2V occurs and V_2 is the voltage of the second extremum and the subband energy spacing is determined only at the gate voltage of coincidence.

Figure 5.19 (a) shows the subbands of the first 1D wire which has 16 subbands at V_{mg} of 0.0 V and a subband spacing, $E_{(0,1)}$, of 2.5 meV. In figure 5.19 (b) shows two clear distinct regions, firstly, the subbands of the first 1D wire and other is the subbands of the mixing region which happens at V_{sg} of -1.5 V. The higher subbands of the first 1D wire starts depopulating and only has 8 subbands left as the 1D wire is moved to the weak confinement regime and the subband spacing of the 1D has reduced to be, $E_{(0,1)}$, 1.9 meV. The mixing regime shows three plateaus

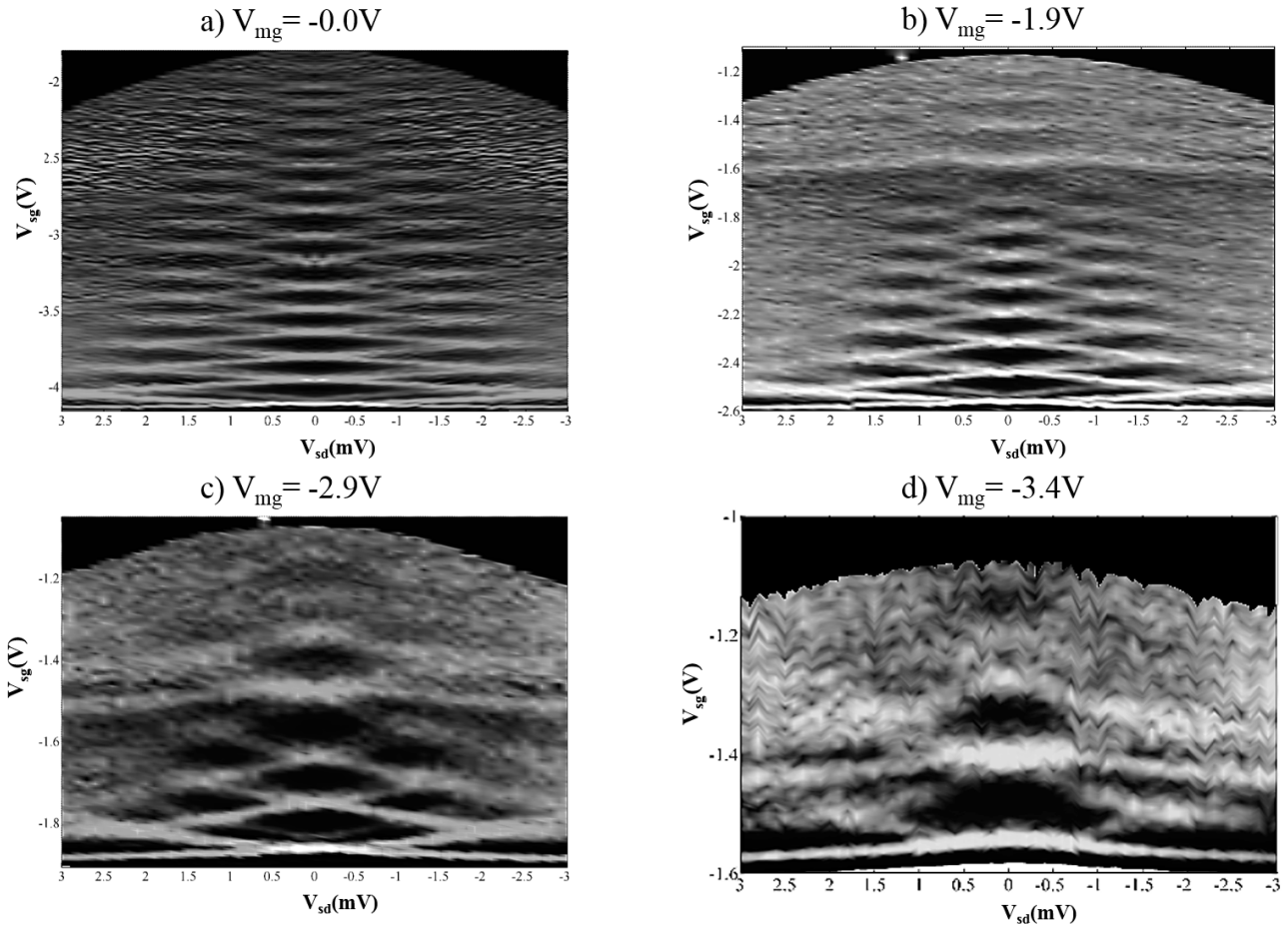

Figure 5.19: Greyscale plot of transconductance of the data in figure 5.6, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

and the subband spacing is around 1.4 meV. In figure 5.19 (c) shows two clear distinct regions, firstly, the subbands of the 1D wire and other is the subbands of the mixing region which happens at V_{sg} of -1.5 V. The higher subbands of the first 1D wire depopulate further and only 3 subbands are left as the 1D wire is moved to a weaker confinement regime and the subband spacing of the 1D has reduced to be, $E_{(0,1)}$, 1.5 meV. The mixing regime shows strengthening of the first plateau and subband spacing is around 1.4 meV. In figure 5.19 (d) shows two distinct regions, firstly, the subbands of the 1D wire and other is the subbands of the mixing region which happens at V_{sg} of -1.4 V. Only one subband of the first 1D wire is present as the 1D wire is moved to a weaker confinement regime and the subband spacing of the 1D is, $E_{(0,1)}$, 1.5 meV. The mixing regime becomes more pronounced and shows strengthening of the plateaus and subband spacing of the double jump is around 1.0 meV. In figure 5.20, dc-bias plots for traces (e) to (g) of figure 5.18 are shown where the dc bias voltage is varied from 3 mV to -3 mV in steps of 0.1 mV. Figure 5.20 (e) shows the subbands spacing of a direct double jump to $\frac{4e^2}{h}$ followed by another jump from $\frac{4e^2}{h}$ to $\frac{6e^2}{h}$ and the subband spacing is estimated to 1.5 meV. This happens when each 1D wire is contributing symmetrically to the 1D conduction and this can be seen by two subbands overlapping at V_{sg} of -1.6 V. Figure 5.19 (f) shows the subbands spacing of a direct double jump to $\frac{4e^2}{h}$ and the subband spacing is estimated to 1.6 meV. Figure 5.19 (g) shows the subbands of the other 1D wire which has 3 subbands and a subband spacing, $E_{(0,1)}$, of 1.0 meV which has a smaller subband than other 1D wire by a factor of 0.5.

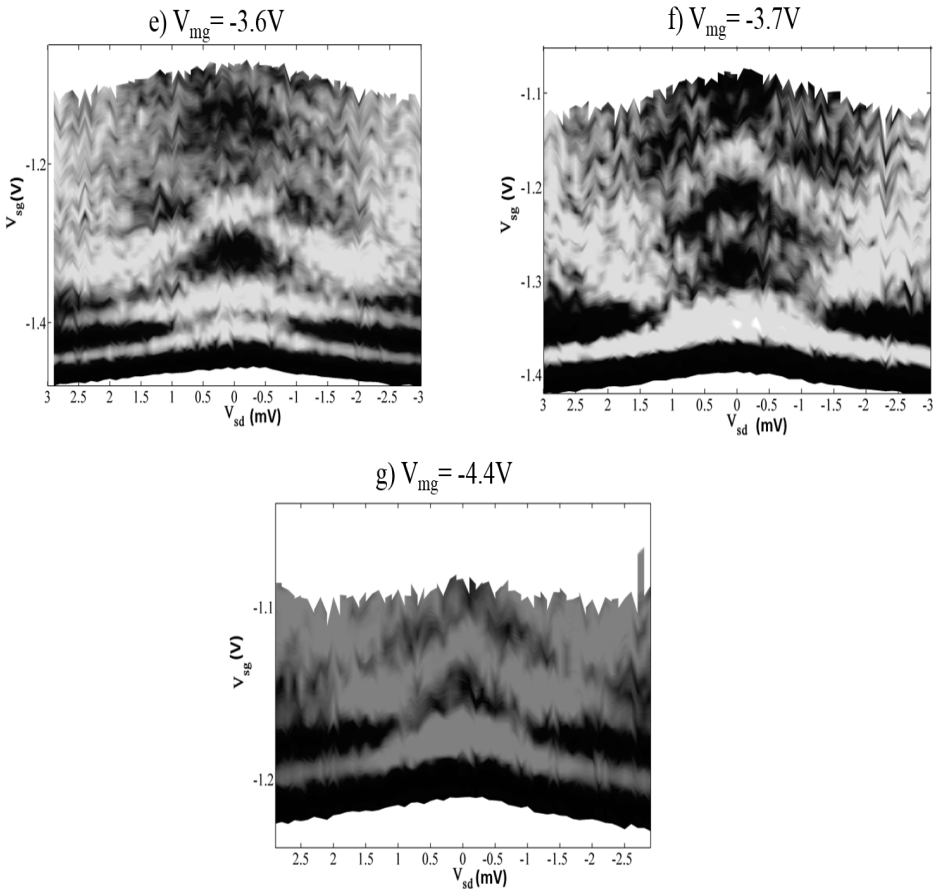

Figure 5.20: Greyscale plot of transconductance, $\frac{dG}{dV_{sg}}$, of the data in figure 5.18 e) to g) as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

5.2.4 ZBA Measurement

A narrow conductance peak called a zero-bias anomaly (ZBA) is observed as the dc source-drain bias, V_{sd}, is swept through zero [123–125]. The ZBA occurs between conductances of zero and $\frac{2e^2}{h}$. At higher temperatures, the ZBA peak reduces and disappears. Cronenwett *et al.* suggested that the formation of a zero-bias conductance peak and the associated enhancement of the peak below

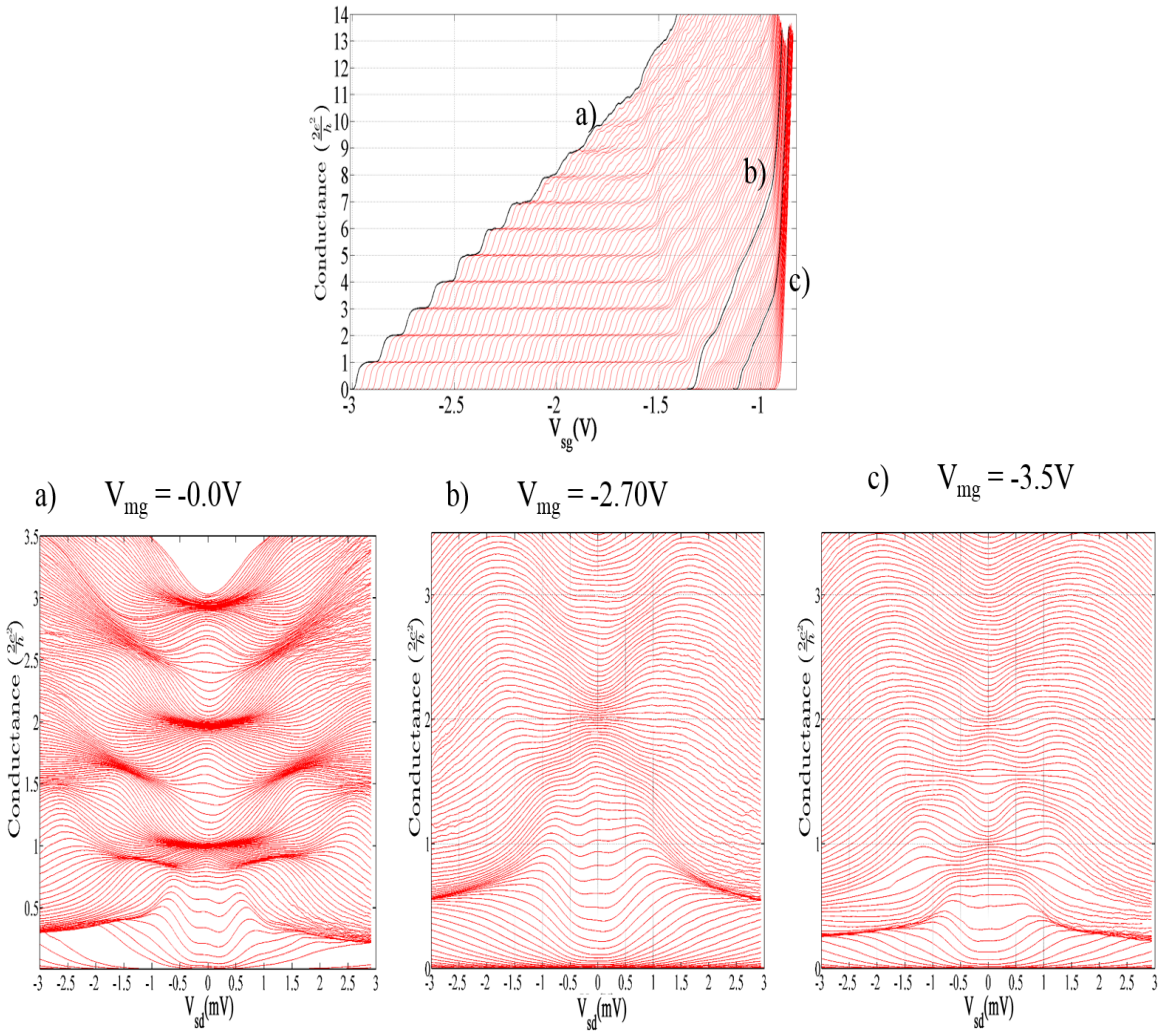

Figure 5.21: a) Differential conductance versus dc bias characteristics in three different regions: a) left-side 1D wire b) mixing regime where a double jump occurs c) right-side 1D. V_{sd} is swept from 3 mV to -3 mV at fixed V_{mg} and V_{sg} and V_{sg} is incremented by 2 mV between traces while V_{mg} remains fixed. a) V_{mg} is fixed at -0.0 V b) V_{mg} is fixed at -2.7 V c) V_{mg} is fixed at -3.5 V.

$\frac{2e^2}{h}$ at low temperatures are similar to the Kondo effect seen in quantum dots [123]. However, Chen *et al.* suggests a simple phenomenological model to explain the occurrence of a ZBA peak when the 1D subband energy rises with increasing

source-drain bias and argue that the Kondo mechanism is not required for zero-bias anomalies to occur in quantum wires [124].

A ZBA measurement was performed in the three distinct regimes of 1D the right-hand 1D wire, the mixing regime and left-hand 1D wire. Figure 5.21 shows the bold and black traces in the three regimes for which the ZBA measurements were performed at various mid-line gates voltages, V_{mg}, 0.0V, -2.7V and 3.5V respectively. V_{sd} is swept from -3 mV to 3 mV at fixed V_{mg} and V_{sg} values and then V_{sg} is incremented between traces by 0.002 V. Figure 5.21 (a) shows the ZBA measurement of left-hand side 1D wire and below $\frac{2e^2}{h}$, a ZBA peak exists which disappears beyond $\frac{2e^2}{h}$. Figure 5.21 (b) shows ZBA in the mixing regime where a jump to $\frac{4e^2}{h}$ occurs where a weak ZBA is present and strengthens up to $\frac{4e^2}{h}$ plateau. In a 1D quantum wire, the ZBA is normally present for all conductances traces below $\frac{2e^2}{h}$ and the double-jump in the mixing regime does not show a simple doubling of the single 1D wire characteristics. Below $\frac{e^2}{h}$ at V_{sd}= 0, the ZBA has disappeared. Figure 5.21 (c) shows ZBA in the left-hand 1D wire where ZBA is suppressed and not present and the ZBA suppression persists across the whole range of confinement. It is interesting to point out that a ZBA was observed in both the left-hand 1D wire and the mixing regime and not seen on the right-hand wire.

5.2.4.1 ZBA Temperature Dependent Measurement

The ZBA measurement was performed again at 500 mK. Figure 5.22 shows the dc-bias measurements as the temperature is increased to 500 mK. As expected, the ZBA peak weakens with increase in temperature and is completely suppressed.

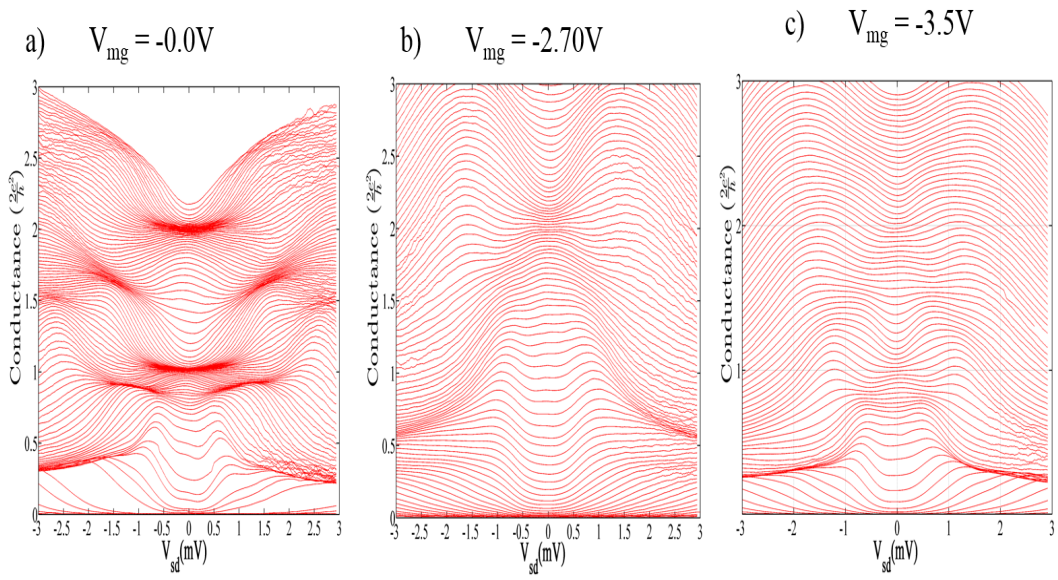

Figure 5.22: Differential conductance versus dc bias characteristics in three different regions at 500 mK: a) left-side 1D wire b) mixing regime where a double jump occurs c) right-side 1D. V_{sd} is swept from 3mV to -3mV at fixed V_{mg} and V_{sg} and V_{sg} is incremented by 2 mV between traces while V_{mg} remains fixed. The mid-line gate, V_{mg}, is fixed at -0.0 V in a). The mid-line gate, V_{mg}, is fixed at -2.7 V in b) and the mid-line gate, V_{mg}, is fixed at -3.5 V in c).

Figure 5.23 shows a detailed temperature study performed in the mixing regime at V_{mg}=-2.7 V where the double jump to $\frac{4e^2}{h}$ occurs. The split-gate voltage, V_{sg}, was fixed at -1.35V where $0.7(\frac{2e^2}{h})$ occurs and the temperature was varied from 20 mK to 1.0K. The ZBA peak gradually weakens as the temperature is increased and the peak is completely suppressed at 500 mK.

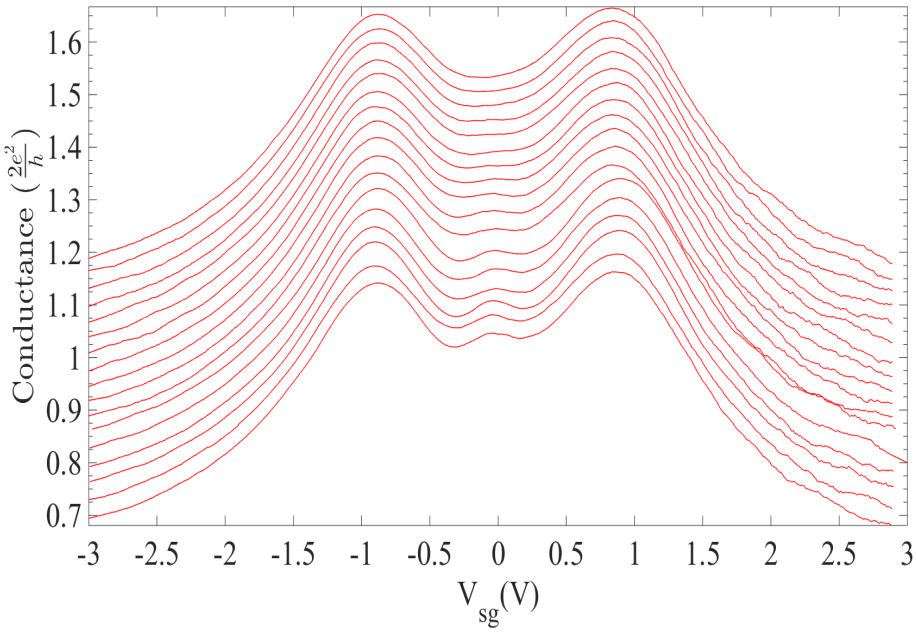

Figure 5.23: a) Differential conductance versus dc bias characteristics in the mixing regime where a double jump occurs. V_{sd} is swept from 3 mV to -3 mV at fixed V_{mg} at -2.7 V and fixed V_{sg} at -1.35V (0.7 structure). The temperature was varied from 20 mK, 50 mK, 100 mK, 150 mK, 200 mK, 250 mK, 300 mK, 350 mK, 400 mK, 450 mK, 500 mK, 600 mK, 700 mK, 800 mK, 900 mK and 1000 mK. The traces are vertically offsetted for clarity and the lowest trace is taken at 20mK.

5.3 Summary

In this chapter a device consisting of split-gates and thin mid-line gates of width of 60 nm was used in an attempt to create two lateral and closely separated 1D wires in a single 2DEG. The differential conductance measurements showed two 1D wires conducting as well as a mixing region in-between those wires. The mixing region showed an addition of both the wires to $4e^2/h$ which indicates that both 1D wires are uncoupled. The different regimes of the differential conductance measurements were explored further by performing subband spectroscopy measurements using a dc-bias technique thus allowing the investigation of subband energies of the adjacent and mixed 1D wires. A detailed study was done to investigate the effect of perpendicular magnetic field on the mixing between the two 1D wires. The application of a perpendicular magnetic field localised the wavefunction of 1D wires thus reducing the overlapping of two 1D wires. Asymmetric voltage bias was applied to the arms of the split-gates device to laterally shift the channel to probe the variation of potential in the channel. The experimental data confirmed that the creation of the two wires is by means of electrostatic effects only and not by an impurity in the channel.

Chapter 6

Wavefunction Hybridisation in Laterally-coupled One-Dimensional Quantum Wires

6.1 Introduction

Mixing of the wavefunctions occurs in a strong coupled device when two 1D wires are closely separated. The coupling between the two 1D wires depends on the interaction and overlap between their wavefunctions. Thomas and Castleton *et al.* measured two strongly coupled 1D quantum wires with a separation between the double quantum wells around 2.5 nm [112–114]. Previously, double quantum well wafer was favoured as it can produce 1D wires that can be much closer together than laterally patterned parallel 1D wires formed in a single 2DEG and therefore provide a good testing ground for investigating interaction effects in one dimension [3, 109, 110, 126, 127]. It is challenging to create two 1D wires closely separated in a single 2DEG by electrostatic gating due to limitations in lithographic resolution [4]. In the present work, a very thin mid-line gate, 20 nm wide, was carefully patterned in an attempt to investigate interaction effects.

6.2 Wavefunction Coupling

The coupling of electrons in two 1D wires can be explained in terms of the wavefunction of individual 1D wires. The potential of 1D constriction can be described as a saddle point where a parabolic barrier in the x direction and a parabolic confinement in y-direction. The two 1D wires are assumed to have two aligned saddle points at the same position (x, y), and their transport properties are determined by the wavefunctions $\Psi_j(x, y, z)$ where $j = u$ or l representing the two 1D wires. The unperturbed wavefunction of each 1D wire are separable and can be expressed as [112, 113]

$$\Psi_j(x, y, z) = e^{ik_x x}\phi_{i,n}(y)Z_{i,n}(z) \tag{6.1}$$

where $n = p$ for $i = u$ and $n = q$ for $i = l$, $\phi_{j,n}(y)$ is nth 1D subband wavefunction and $Z_{i,n}(z)$ is the wavefunction of ground state of the quantum well and it is dependant on the 1D subband index n. A peak in dG/dV_{sg} occurs at $k_x = 0$ and the matrix that determines the mixing between subbands p and q of 1D wires u and l respectively can be expressed [112, 113]

$$\langle \Psi_u | V_z | \Psi_l \rangle = \int \phi_{u,p}(y)\phi^*_{l,q}(y)dy \int Z_{u,p}(z)V(z)Z^*_{l,q}(z)dz \tag{6.2}$$

where $V(z)$ is the conduction band profile of the quantum well. The coupling between the two wavefunctions is determined by the integral

$$I = \int \phi_{u,p}(y)\phi^*_{l,q}(y)dy \tag{6.3}$$

when the integral I is zero, the 1D subbands p and q cross without mixing. The alignment of the two 1D wires and symmetries of their wavefunctions influences the integral I. When the two 1D wires are misaligned, $I \neq 0$, there will be complicated mixing of the entire subbands of the two wires. When the two 1D wires are aligned and have the same width, $I = \delta_{p.q}$, the y and z components of the unperturbed wavefunctions mix when $p = q = n$ to give the bonding and anti-bonding states. The bonding wavefunction can be expressed [112, 113]

$$F_n(y,z) = \frac{1}{\sqrt{1+\beta^2}}[\phi_{l,n}Z_{l,n}(z) + \beta\phi_{u,n}(y)Z_{u,n}(z)] \tag{6.4}$$

and anti-bonding wavefunction can be expressed as

$$F_n(y,z) = \frac{1}{\sqrt{1+\beta^2}}[\phi_{l,n}Z_{l,n}(z) - \phi_{u,n}(y)Z_{u,n}(z)] \tag{6.5}$$

where β is constant describing the extent of the wavefunction is in each wire and is determined by the position along the axis of the 1D wire which is a linear combination of the split-gates voltages, V_{sg}, and the mid-line gate, V_{mg}. When the 1D wires are at resonance ($\beta = 1$), the energy gap, Δ^n_{SAS}, between the symmetric and antisymmetric 1D subbands at their anti-crossing is given by the integral

$$\Delta^{n}_{SAS} = 2\int Z_{u,p}(z)V(z)Z^{*}_{l,q}(z)dz \tag{6.6}$$

At $B = 0$ the integral $I = \delta_{p,q}$, there is only mixing between subbands of the same index. Applying an in-plane magnetic field will introduce a relative shift of the two 1D wires wavefunctions in k_y-space by an amount $\delta k_y = eBd/\hbar$ where d is the tunnelling distance between the 1D wires in the z-direction and the overlap integral can be written as [112, 113]

$$I = \int \widetilde{\phi}_{u,p}(k_y - eBd/\hbar)\widetilde{\phi}^{*}_{l,q}(k_y)dk_y \tag{6.7}$$

where $\widetilde{\phi}_{j,p}(k_y)$ is the Fourier transform of $\phi_{j,p}(y)$. Applying an in-plane magnetic field alters the integral ,I, and mixing between subbands of different index occurs and hence anti-crossings.

6.3 Subband Energy locking

When a pair of energy levels of a system approach another similar system, a perturbation occurs causing the system to couple leading to energy levels either to cross or anti-cross as seen in figure 6.1 (a) and (b) respectively [128]. Anti-crossing of energy levels occur as a result of quantum hybridisation between the two subsystems and crossing of energy levels occurs when the Hamiltonian matrix responsible for the hybridisation vanish due to symmetry.

The hybridisation of the energy subbands opens an energy gap causing the

lifting of the energy level and this gap can be expressed as δ_{SAS} and can be seen in figure 6.1 (b). Sun *et al.* proposed a third possibility arising when adjacent energy levels lock together instead of repelling each other and it can be seen in figure 6.1 (c) [5]. The energy levels lock when the energy level cross near the Fermi level leading to a charge imbalance occurring and the energy levels lock together.

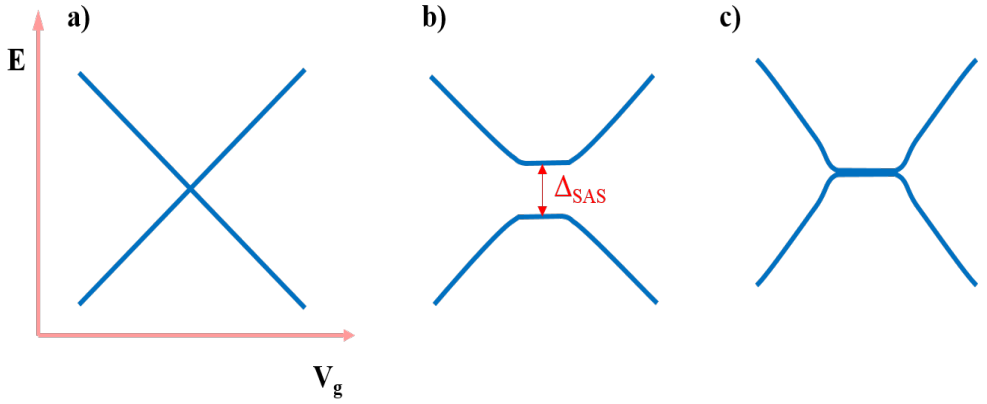

Figure 6.1: A schematic diagram of the energy levels in a system of two conductors as a function of gate voltage where levels may cross a), anti-cross b) or lock c). The figure has been adapted from ref [5].

6.4 Experimental Methods

6.4.1 Wafer Details

The devices used in this chapter were fabricated on a delta doped GaAs/$Al_xGa_{1-x}As$ heterostructures. The two-dimensional electron gas is located 286 nm below the surface, with electron density, n_{2d}, $2.2 \times 10^{11} cm^{-2}$ and mobility μ of $7.95 \times 10^6 cm^2/Vs$ and further details of the wafer used, W731, is given in appendix A.

6.4.2 Device Fabrication

Split-gate devices with a thin mid-line gate were drawn using electron-beam lithography and Ti/Au was deposited to form Schottky gates. The split-gates device in the present work has a length of 400 nm and width of 700 nm and the mid-line gate has a width of 20 nm. the mid-line gate can control the electron density in the 1D wire. A strong negative bias on the mid-line gate could divide the channel into two lateral 1D wires and if the width of the mid-line gate is thin, it may allow interactions between the two 1D wires. In addition, a 300 nm dielectric layer of cross-linked PMMA was deposited on the channel below the track and the optical gate of the mid-line gate. Figure 6.2 shows an optical image of the mid-line gate in between the split-gates with cross-linked PMMA deposited underneath the tracks connecting the mid-line gates.

6.5 Results

This section addresses a more comprehensive study of the interactions effects in laterally coupled quantum wires showing the crossing and anti-crossing of the 1D subbands.

6.5.1 Mid-line Gate Characteristics

The main result in this chapter is the formation of a coupled horizontally aligned pair of 1D wires in a single 2DEG. Figure 6.3 shows two-terminal conductance G=dI/dV plot where the mid-line gate voltage, V_{mg}, was varied from 0.0 to -6.0 V in -30 mV steps. The split-gates voltage, V_{sg}, defines the 1D quantum

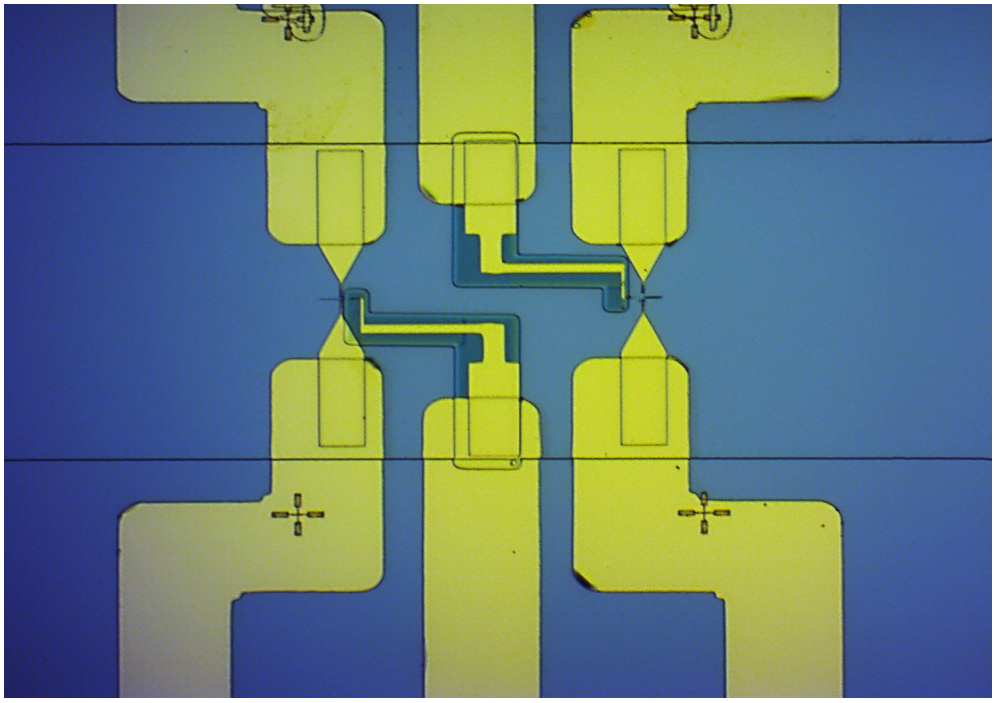

Figure 6.2: An optical image of the split-gates devices with a 20 nm wide mid-line gate.

wire and as V_{mg} becomes more negative the subbands in the right-side side wire are depopulated first. There are three distinct regions that are observed. The regions at the right side and bottom left arise from a single quasi-1D channel on either sides of the mid-line gate. Both 1D wires exhibit clean quantised ballistic conductance plateaus in steps of $\frac{2e^2}{h}$. In the mixed region, complicated structures occur where 1D subbands of the two wires become nearly degenerate. In the mixed region, the 1D wires are present and conduct with a total conductance equal to the sum of the conductance of each wire. There is a smooth transition of conduction from one 1D wire to other while maintaining the ballistic conductance. Therefore by varying V_{sg} and V_{mg}, the fraction of the current passing through both 1D quantum wires can be tuned. Figure 6.4 shows a blow up of figure 6.3 at

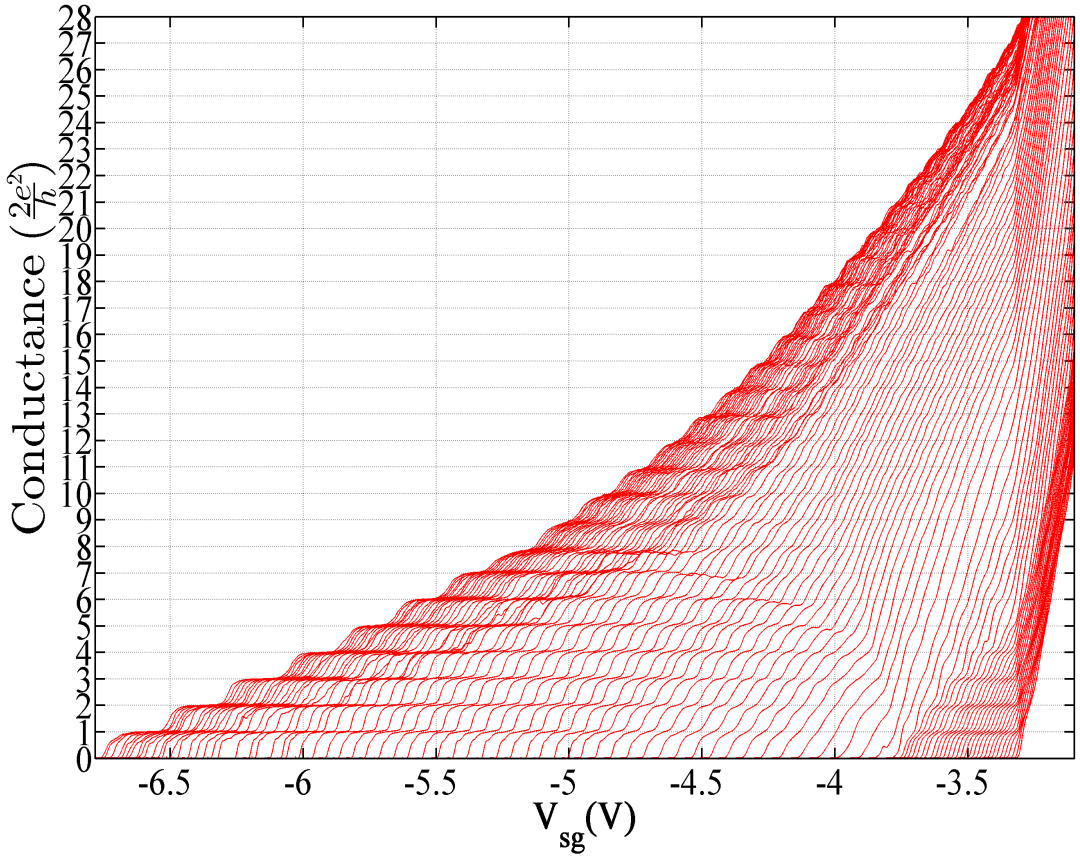

Figure 6.3: Conductance data from a mid-line gated device at T = 10 mK and electron temperature of $\sim$ 70 mK. For each trace V_{sg} is swept and V_{mg} is fixed. V_{sg} is incremented in steps -30 mV intervals from 0.0 V on the left to -6.0 V on the right. The split-gates have dimensions of 400 nm in length and 700 nm in width, with a 20 nm wide mid-line gate.

the mixing region to show a more detailed picture of the crossing and ant-crossing of both 1D wires.

To understand the conductance characteristics better, figure 6.3 is differentiated with respect to V_{sg} to produce a grey-scale plot shown in figure 6.5. The black lines correspond the transconductance $\frac{dG}{dV_{sg}}$ maxima between plateaus indicating where a 1D sub-band edge crossing through the chemical potential. The

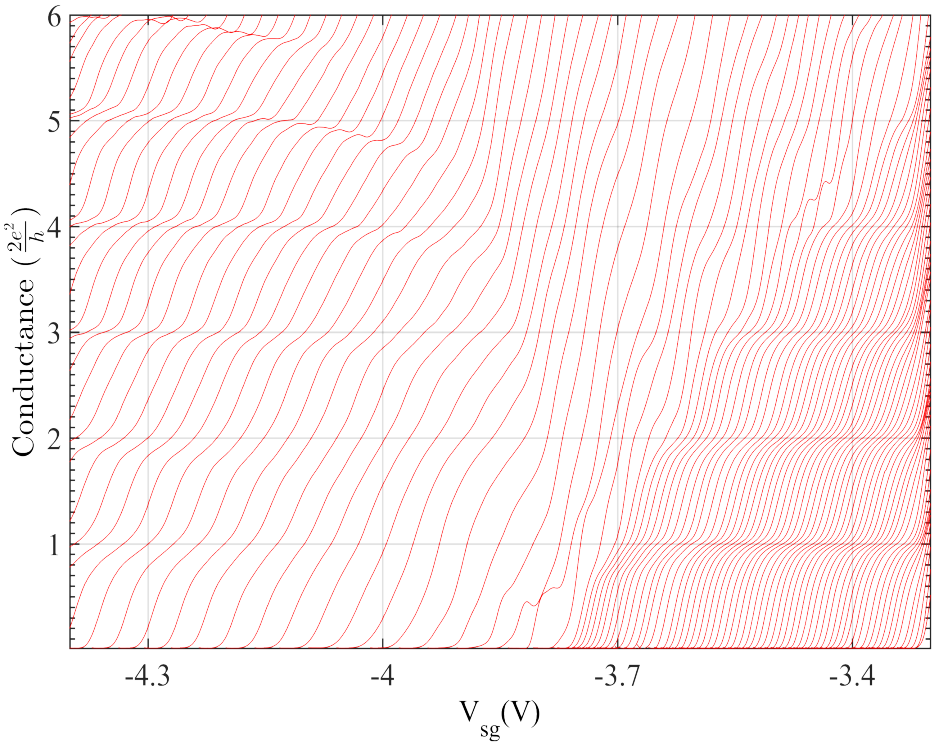

Figure 6.4: A blow up of the conductance data of figure 6.3 at the mixing region of the 1D wires where both wire cross. For each trace V_{sg} is swept and V_{mg} is fixed. V_{sg} is incremented in steps -30 mV intervals. The split-gates have dimensions of 400 nm in length and 700 nm in width, with a 20 nm wide mid-line gate.

1D sub-band edges are therefore represented by the grey lines. The left-side and right-side side shows the 1D sub-bands edges of each 1D wire. The mixing region in-between shows the crossing of 1D subbands from each wire and in the overlapping region, the two 1D wires are strongly coupled and the 1D sub-bands in the both wires cross. It may also be noted that just before the two 1D wires cross, the ground state and the first excited state of the left side 1D wire anti-cross, as indicated by a blue arrow in figures 6.5 and 6.6. Figure 6.6 shows a blow up of

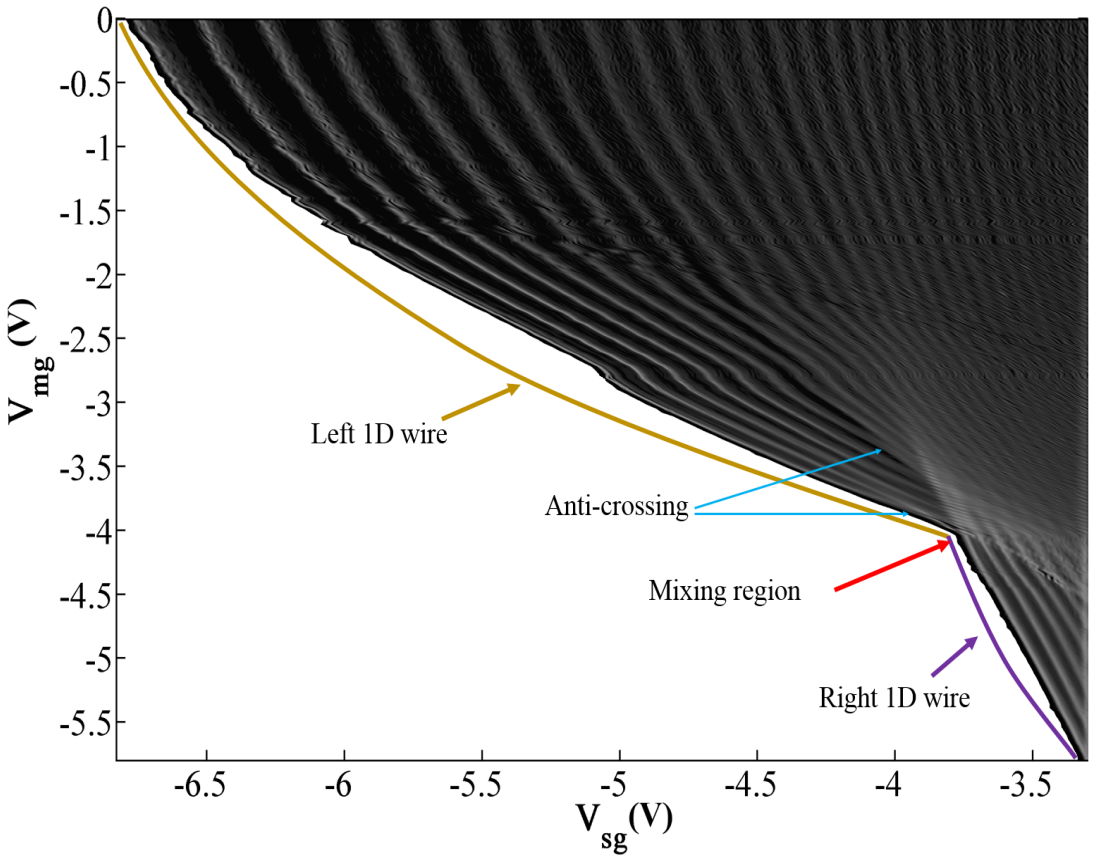

Figure 6.5: Grey-scale plot of transconductance of the data in figure 6.3, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

figure 6.5 at the transition where two 1D wires cross with each other. In addition, Thomas and Castleton *et al.* measured mid-line gated devices on DQW where the $Al_xGa_{1-x}As$ barrier was 2.5 nm and in these devices the 1D wires in each well were strongly coupled, and showed that the 1D sub-bands in the both wires anticrossed [4, 112].

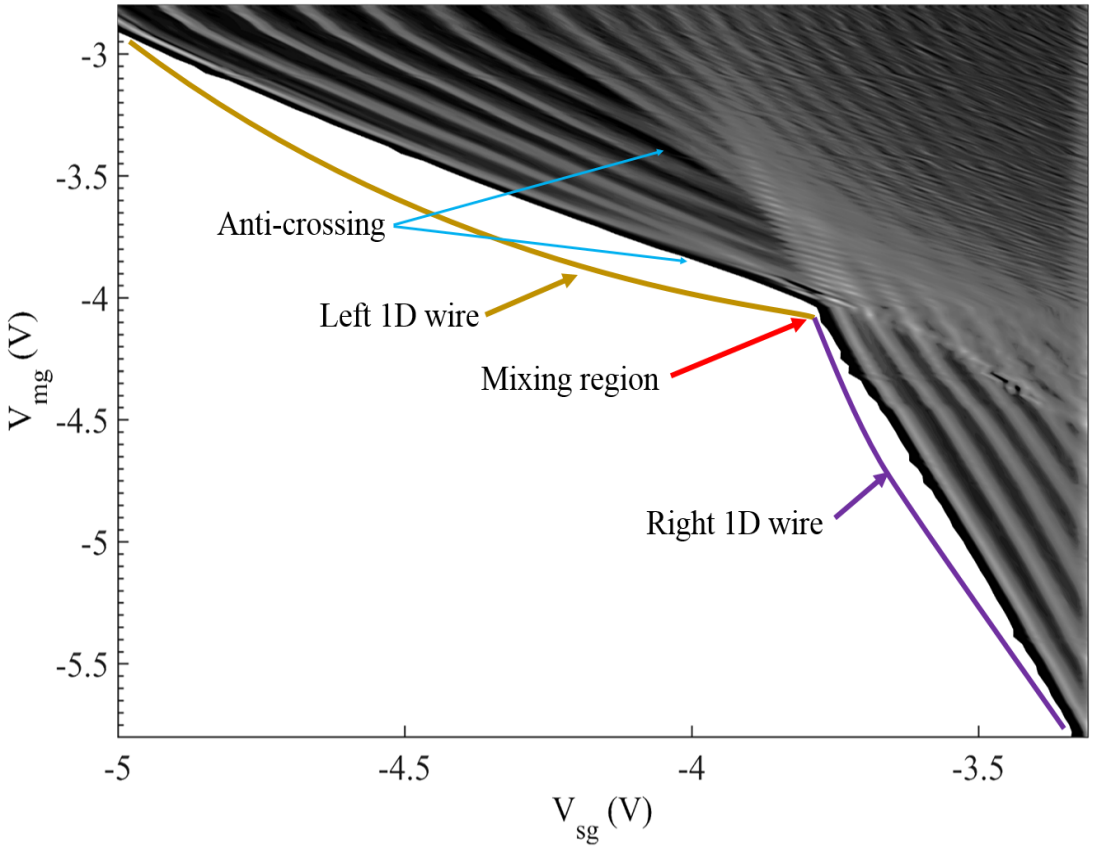

Figure 6.6: A blow up of the greyscale plot in figure 6.5, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg} at the transition where two 1D wires conduct simultaneously in steps of $\frac{4e^2}{h}$. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

6.5.2 Laterally-Shifting the channel

An asymmetric voltage bias can be applied to split-gates to laterally shift the 1D wire [118, 119]. This technique can be used to laterally shift the 1D wire to probe the variation of potential in the channel or to move the 1D wire away from a disorder. In this section, the conductance is measured by applying offset voltages on one arm of the split-gates and sweep both split-gates together.

6.5.2.1 Laterally Shifting the 1D Channel

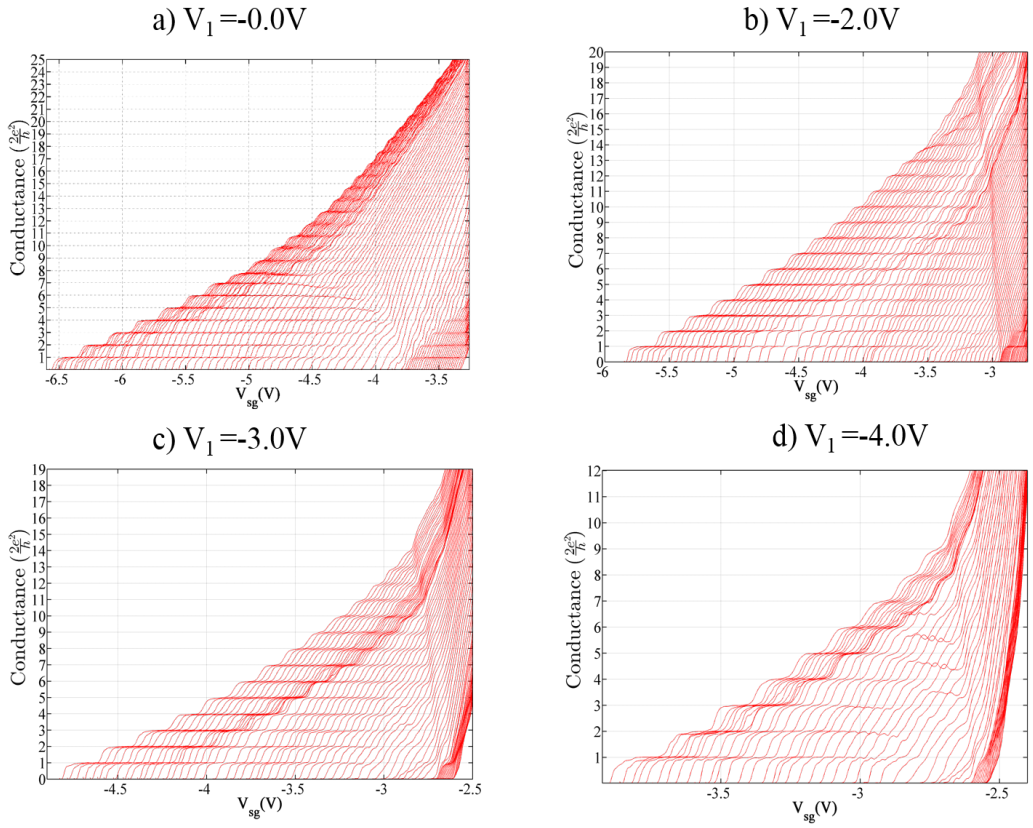

Figure 6.7: Conductance characteristics of the sample as the 1D channel is shifted laterally. The conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -60 mV in all the plots. In a) the 1D channel has no offset applied between the arms of the split-gates. In b), the channel is shifted by applying an offset of -1.0 V. In c) the channel is shifted with an offset of -3.0 V. In d) the offset is increased to -4.0 V.

Figures 6.7 a) to d) show the conductance characteristics of the sample for different bias voltages applied on one arm of the split-gates. Figures 6.8 a) to d) show the blow up of the conductance characteristics of the sample at the mixing regeime of figure 6.7. Figure 6.7 a) shows when no asymmetric bias is applied and

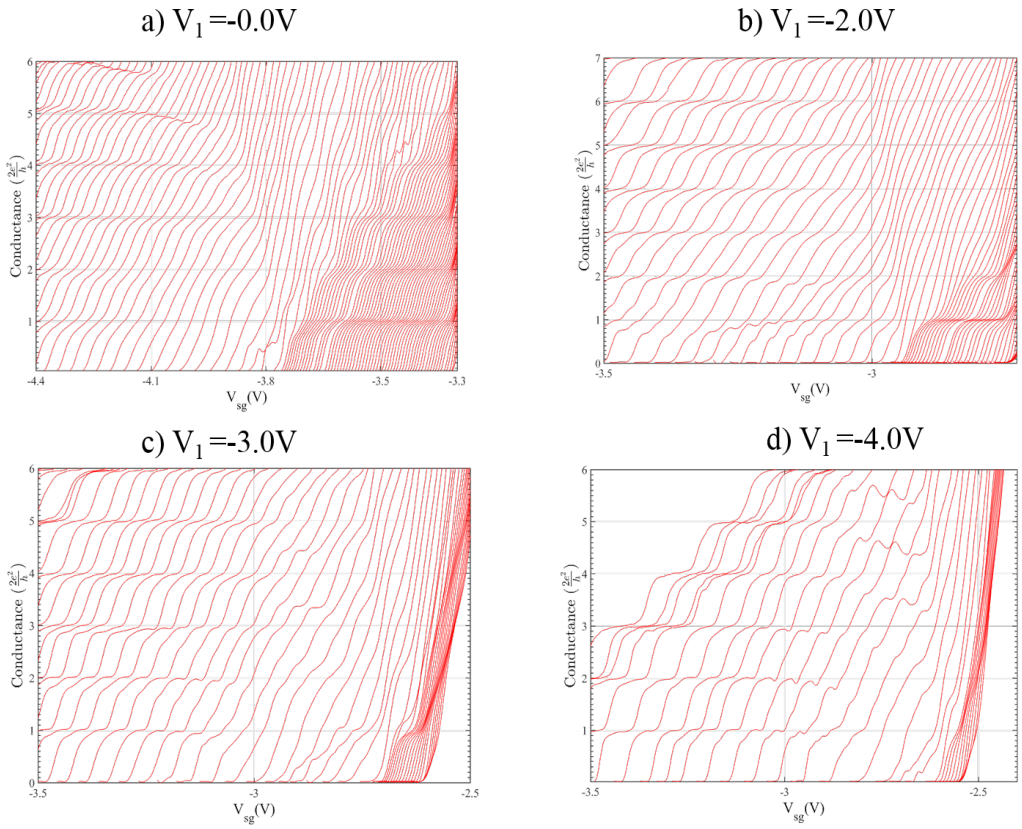

Figure 6.8: The blow up of the conductance characteristics of figure **??** at the mixing regime. The conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -60 mV in all the plots. In a) the 1D channel has no offset applied between the arms of the split-gates. In b), the channel is shifted by applying an offset of -1.0 V. In c) the channel is shifted with an offset of -3.0 V. In d) the offset is increased to -4.0 V.

V_{mg} is stepped from 0.0 V on the left to -5.9 V on the right in intervals of -60 mV. In figure 6.7 b) an offset of -2.0 V is applied on one arm, V_1, which laterally shifts the 1D channel in one direction. In figure 6.7 c) the channel is shifted by -3.0 V. The channel is shifted further in the same direction and in figure 6.7 d) where an offset of -4.0 V is applied. It is important to notice that the plateaus are well defined and do not change in length reflects no change in the subband spacing

due to the asymmetric bias. As the left arm is incremented by a negative offset ,V_1, by -2.0 V, the higher plateaus of the right-side 1D quantum wire disappear, leaving only two plateaus in the 1D wire and the mixing regime has also decreased. The arm of the split-gates is incremented further by a negative offset ,V_1, of -3.0 V, resulting in the second plateau disappearing in the right-side 1D quantum wire, leaving only one plateau in the 1D wire which results in the mixing regime reducing further. The arm of the split-gates is incremented further by a negative offset ,V_1, of -4.0 V, resulting in the weakening of the first plateau in the right-side 1D quantum wire and also the higher subbands of left-side 1D quantum wire disappear which results in the mixing regime being reduced further.

Figure 6.9 shows a detailed greyscale plot of the data shown in figure 6.7 where a negative asymmetric voltage is applied on the left arm of the split-gates ,V_1, from -1.0 V to -4.0 V. The higher subbands of the right-side 1D wire starts disappearing gradually as the asymmetric voltage, V_1 is increased negatively. However, the right side 1D wire does not disappear completely by applying an offset of -4.0 V. The mixing region disappears progressively as the asymmetric voltage, V_1, is increased up to V_1= -4.0 V. The right-side wire has its crossing with the second wire enhanced as V_1 is increased to -2.0 V as shown in figure 6.9 (b). when V_1 is -3.0 V, the left-side 1D wire has its subbands decreasing further also the mixing region shows clear crossing of the 1D subbands of both wires. When V_1 is -4.0 V, only subbands in the left-side 1D wire are present and the right 1D wire shows a single plateau representing its ground state.

In figure 6.9 (a) when no offset is applied then the right and left wires cross with each other. The right wire has 5 subbands resolved and the left one has more than 10 subbands resolved. The two wires meet and mix at $V_{mg} \sim$ -4 V.

On application of bias voltage of -2 V, see figure 6.9 (b), the number of subbands in the right wire has reduced to 2 (compare to 5 when no bias was present). These two subbands then cross through all the subbands of the left wire. On increasing the bias further to -3V as shown in figure 6.9 (c), only the first subband of the right wire is crossing with the subbands of the left wire. It is noted that the crossing between both the wires could be reduced significantly on applying a significantly large offset of say -4 V[Figure 6.9 (d)].

6.5.2.2 Laterally Shifting 1D Channel in the Reverse Direction

The 1D channel was laterally shifted in the opposite direction by applying a positive asymmetric voltage on the other arm of the split-gates, V_2. A positive voltage was applied to the right arm of split-gates, V_2. Figures 6.10 (a) to (d) show the conductance characteristics of the sample for different positive asymmetric voltages applied on the right-side arm of the split-gates. Figure 6.10 (a) shows a symmetric bias is applied and V_{mg} is stepped from 0.0 V on the left to -6.0 V on the right in intervals of -30 mV. In figure 6.10 (b) an offset of 1.0 V is applied, which laterally shifts the 1D channel in the other direction. In (c), the channel is shifted by 3.0 V. The channel is shifted further in the same direction (d) where an offset of 4.0 V is applied respectively. It is important to note that the plateaus are well defined and change in length at higher asymmetric voltages which reflects change in the subband spacing. When no asymmetric voltage is applied, the left-side 1D wire shows twenty four plateaus and as the right arm is incremented by a positive offset of $V_2 = 1$ V, the higher plateaus of the left-side 1D quantum wire disappear, leaving only nineteen plateaus in the 1D wire and the mixing regime has also decreased. The arm of the split-gates is incremented further by

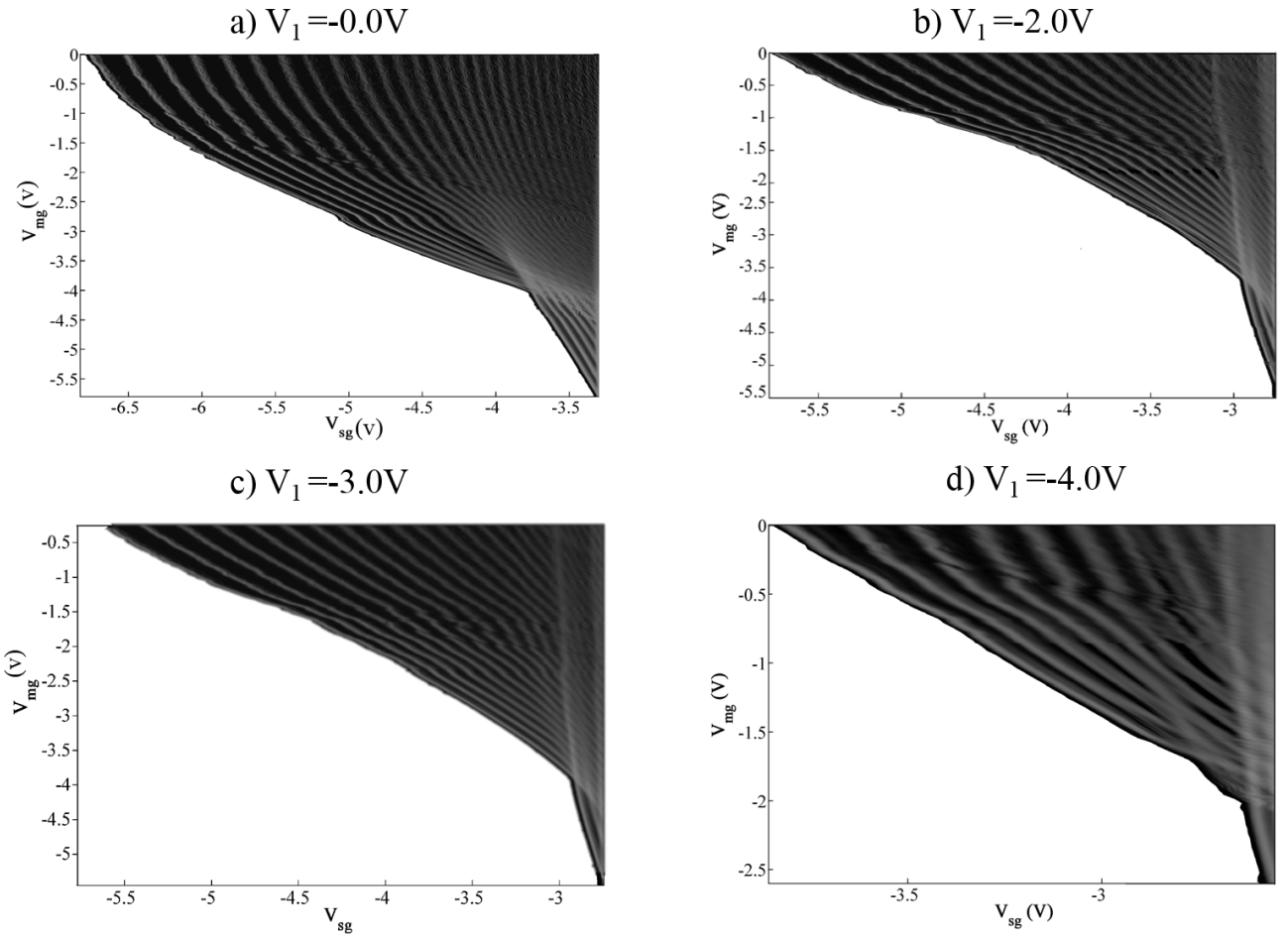

Figure 6.9: Greyscale plot of transconductance of the data in figure 6.9, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

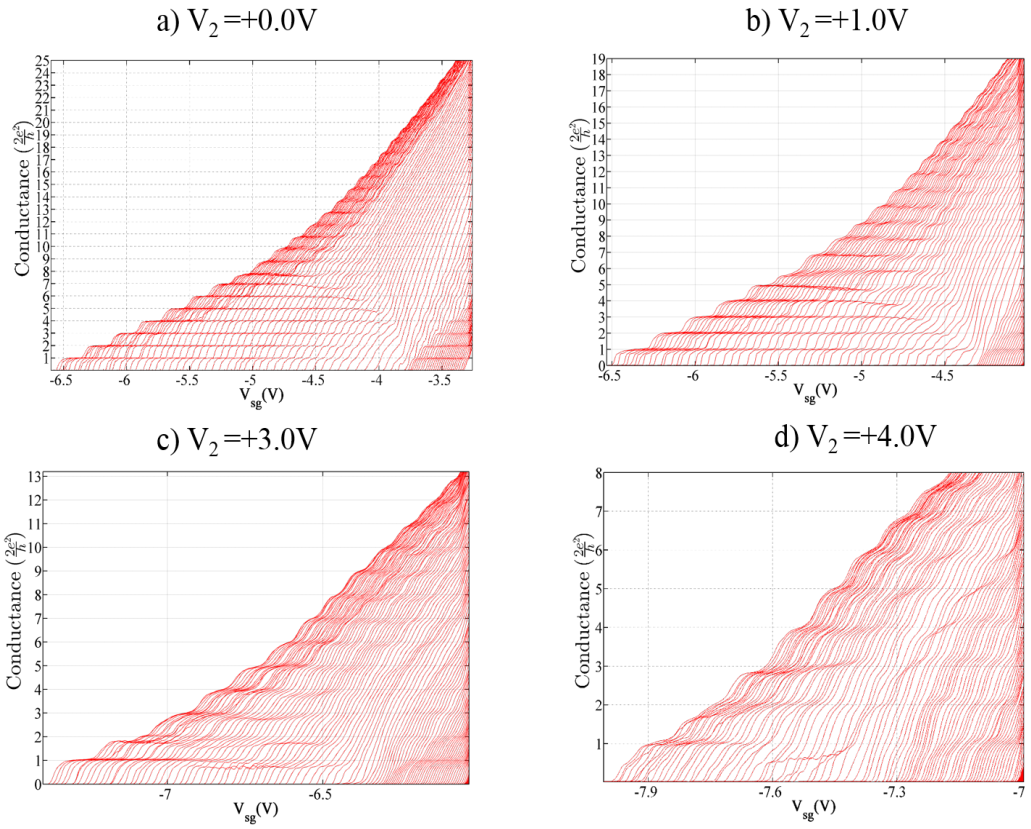

Figure 6.10: Conductance characteristics of the sample as the 1D channel is shifted laterally. The conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -60 mV in all the plots. In a) the 1D channel has no offset applied between the arms of the split-gates. In b), the 1D channel is laterally shifted by applying an offset of 1.0 V between the arms of the split-gates. In c) the channel is shifted with an offset of 3.0 V. In d) the offset is increased to 4.0 V.

a positive offset, V_2, of 3.0 V, resulting in the higher plateaus of the left-side 1D quantum wire disappearing further, leaving only thirteen plateaus in the 1D wire and the mixing regime has also reduced further. The arm of the split-gates is incremented further by a positive offset, V_2, of 4.0 V, resulting in the higher plateaus of the left-side 1D quantum wire disappearing further, leaving only eight

plateaus in the 1D wire and the mixing regime has also reduced further. There are five subbands in the right-side side 1D wire and remain mostly unchanged by the asymmetric voltages that is applied. However, when a positive offset more than 3 V was applied, the subband spacing of the left-side 1D wire changes and the plateaus become less well defined.

To examine the behaviour of laterally shifting the 1D wire in the channel further, the data was differentiated, $\frac{dG}{dV_{sg}}$, and a greyscale plot of transconductance of the data in figure 6.10 was produced. Figure 6.11 shows a detailed greyscale plot of data shown in figure 6.10 where a positive asymmetric voltage is applied on the left arm of the split-gates, V_2, from 0.0 to 4.0 V. The higher subbands of the left-side 1D wire starts disappearing gradually as the asymmetric voltage, V_2, is increased and this confirms that the creation of the two wires is by means of electrostatic effects only. However, the 1D wire does not disappear completely by applying an offset of 4.0 V. The mixing region weakens progressively as the asymmetric voltage is increased and disappears when V_2 is 4.0 V. The right-side wire has its second and third subbands anti-crossing and also the left-side wire has its third and fourth subbands anti-crossing in figure 6.11 (b) when V_2 is 1.0 V and also anti-crossing of the subbands starts to appear in the mixing region. When V_2 is 3.0 V, the crossing of both 1D wires decreases further and is replaced by anti-crossing at the mixing region. When V_2 is 4.0 V, the crossing of both 1D wires disappears completely and a clear anti-crossing of the first and second subband is happening at the mixing region. In conclusion, laterally shifting the 1D wire using a negative voltage results in crossing of subbands between the 1D wires while a positive voltages results in anti-crossing of subbands between the 1D wires as shown in figure 6.11 and figure 6.9 respectively.

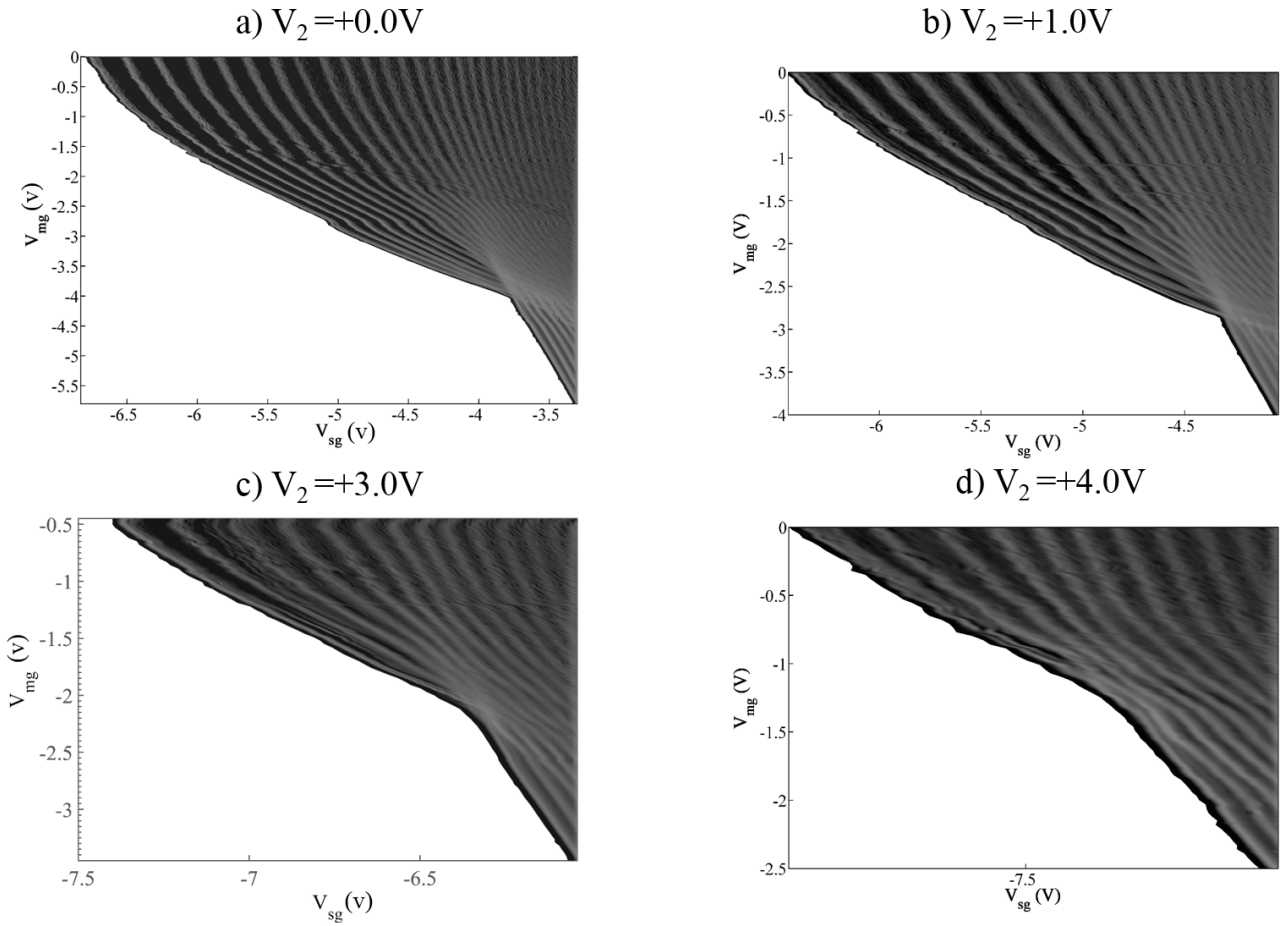

Figure 6.11: Greyscale plot of transconductance of the data in figure f 6.9, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

6.5.3 Source-Drain Bias

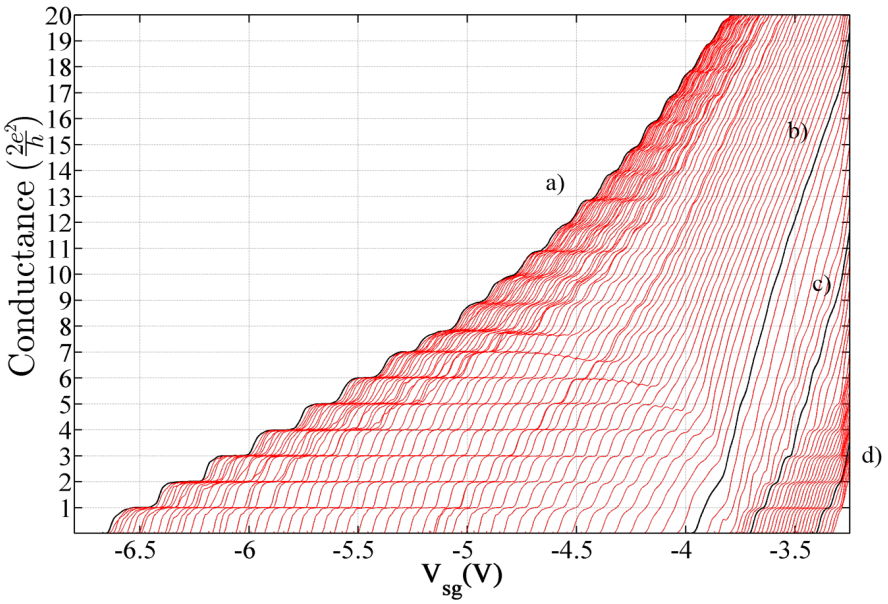

Figure 6.12: Conductance characteristics of the 1D channel and the conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -50 mV in all the plots. The bold, black traces from left to right correspond to sub-band spectroscopy performed in different regions of 1D wire where different mid-line gate voltages, V_{mg}, have been applied; a) V_{mg} =-0.0 V, b) V_{mg} =-2.56 V, c) V_{mg} =-3.18 V and d) V_{mg} =-3.46V.

The energy subbands of a 1D wire can be examined using finite bias across the quantum wire. The differential conductance $G = dI/dV_{sd}$ with a finite dc source-drain bias voltage, V_{sd}, is measured where an ac signal superposed with a dc source-drain bias voltage was applied. Sub-band spectroscopy measurements were performed along the spectrum of the 1D regime from strong confinement to the weak confinement. Figure 6.12 shows the traces selected for dc bias measurement in the regions of left-side 1D wire, the mixing regime and right-side 1D wire by

varying the mid-line gate voltages.

Figure 6.13 shows the greyscale of the dc-bias measurements of traces (a) to (d) shown in figure 6.12 where the dc bias voltage of 3 to -3 mV in steps of 0.1 mV is applied between source and drain of the device. Figure 6.13 (a) shows the subbands of the first 1D wire which has 20 subbands at V_{mg} of 0.0 V and a subband spacing, $E_{(0,1)}$, of 2.5 meV. In figure 6.13 (b) shows the subband spectroscopy at a direct double jump to $4e^2/h$ and there are two clear distinct regions, firstly, the subbands of a direct double jump to $4e^2/h$ and the other is the subbands of the mixing region and this transition happens at V_{sg}= -3.4 V and V_{mg}= -2.56 V. The subband spacing, $E_{(0,1)}$, of the direct double jump is estimated to be around 0.9 meV. Figure 6.13 (c) shows the subbands of the right-side 1D wire which has 3 subbands and a subband spacing, $E_{(0,1)}$, of 1.5 meV which is smaller than left-side 1D wire by a factor of 0.6. There are still two clear distinct regions, firstly, the subbands of the other 1D wire and other is the subbands of the mixing region which happens at V_{sg} of -3.1 V. The mixing region has a subband spacing of 0.3 meV which is considerably smaller than the individual 1D wires, indicating that subbands in the mixed regime are very close to each other. Figure 6.13 (d) shows the subbands of the right-side 1D wire which has 2 subbands and a subband spacing, $E_{(0,1)}$, of 1.1 meV as 1D wire is more into the weakly confined regime. The other subbands observed for V_{sg} = -3 V are due to 1D-2D transitions in the definition regime.

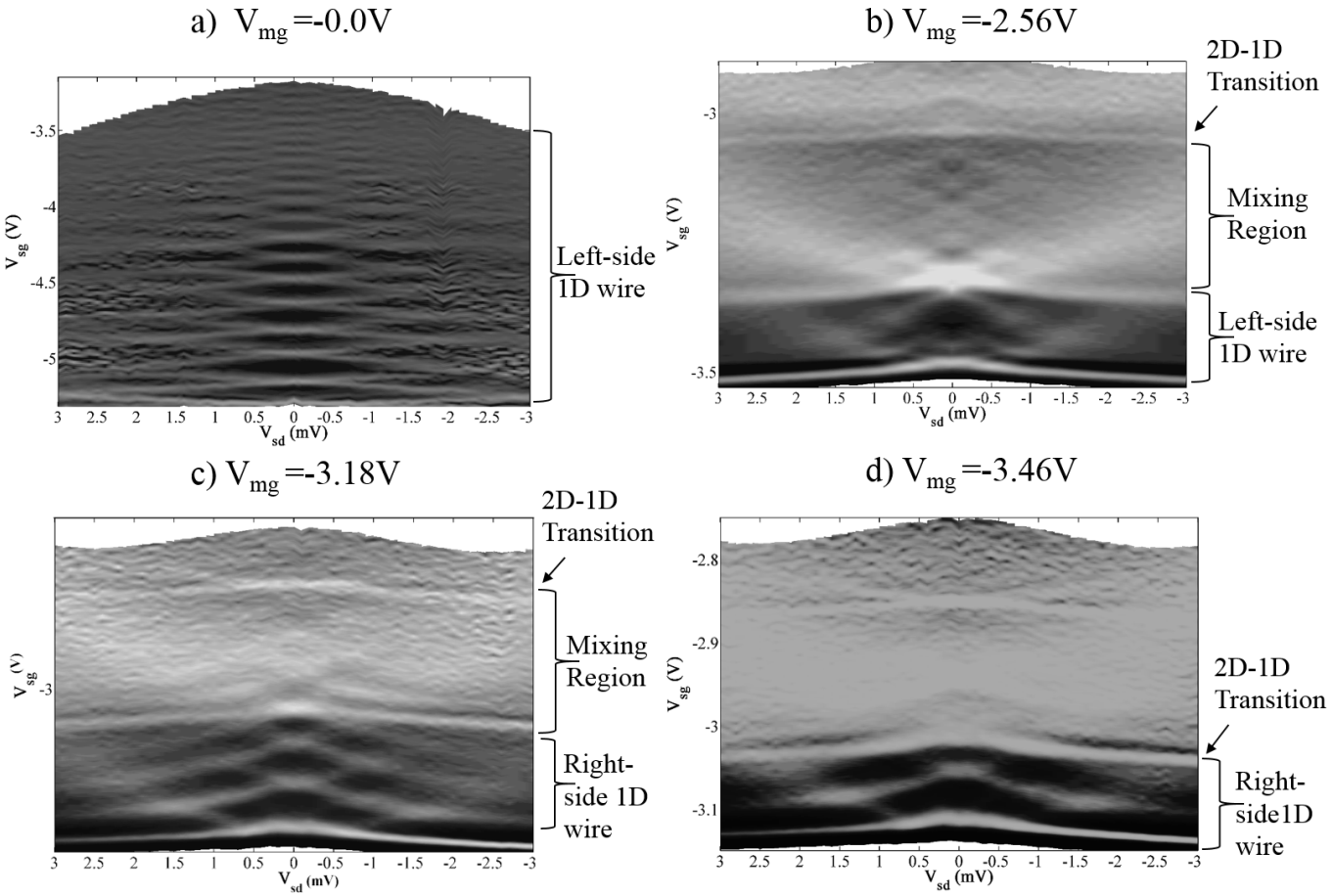

Figure 6.13: Greyscale plot of transconductance of the data in figure 6.9, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

6.5.4 Temperature Dependence

Figure 6.14 shows the temperature dependence of a conductance traces shown in figure 6.3. The conductance of two 1D wires are suppressed as the temperature increases, until it is smeared out to thermal averaging around T $\approx$ 3.0 K. It may be noted that the conductance values of the higher plateaus weaken faster with increasing the temperature. At the mixing region where the crossing and anti-crossing occur, the features smeared out rapidly with increasing the temperature and disappear at T $\approx$ 500 mK on the account of thermal smearing. The small sub-band energy spacing of the anti-crossing is weak and the plateau disappears in the mixing regime so quickly with temperature may be indicative of the fragility of crossing and anti-crossing system. Figure 6.15 shows the greyscale plot of transconductance of the data in figure 6.14 and the interactions effects in the mixed region smears out quickly as the temperature is increased. The three distinct regions in the greyscale representing both 1D wires and mixed wires regimes stay the same as the temperature is increased to 3.0 K indicating that these regions are created due to electrostatic confinement rather than the interaction effects. However, it is worth mentioning that the hybridisation of the ground state and the first excited state in the 1D is temperature dependent as this hybridisation was found to smear out when the temperature exceeded 500 mK.

6.5.5 Density Dependent Measurements

Raising the carrier density of the 2DEG can be achieved by illuminating the sample using a red LED with a wavelength of 650 nm and thus raising the carrier

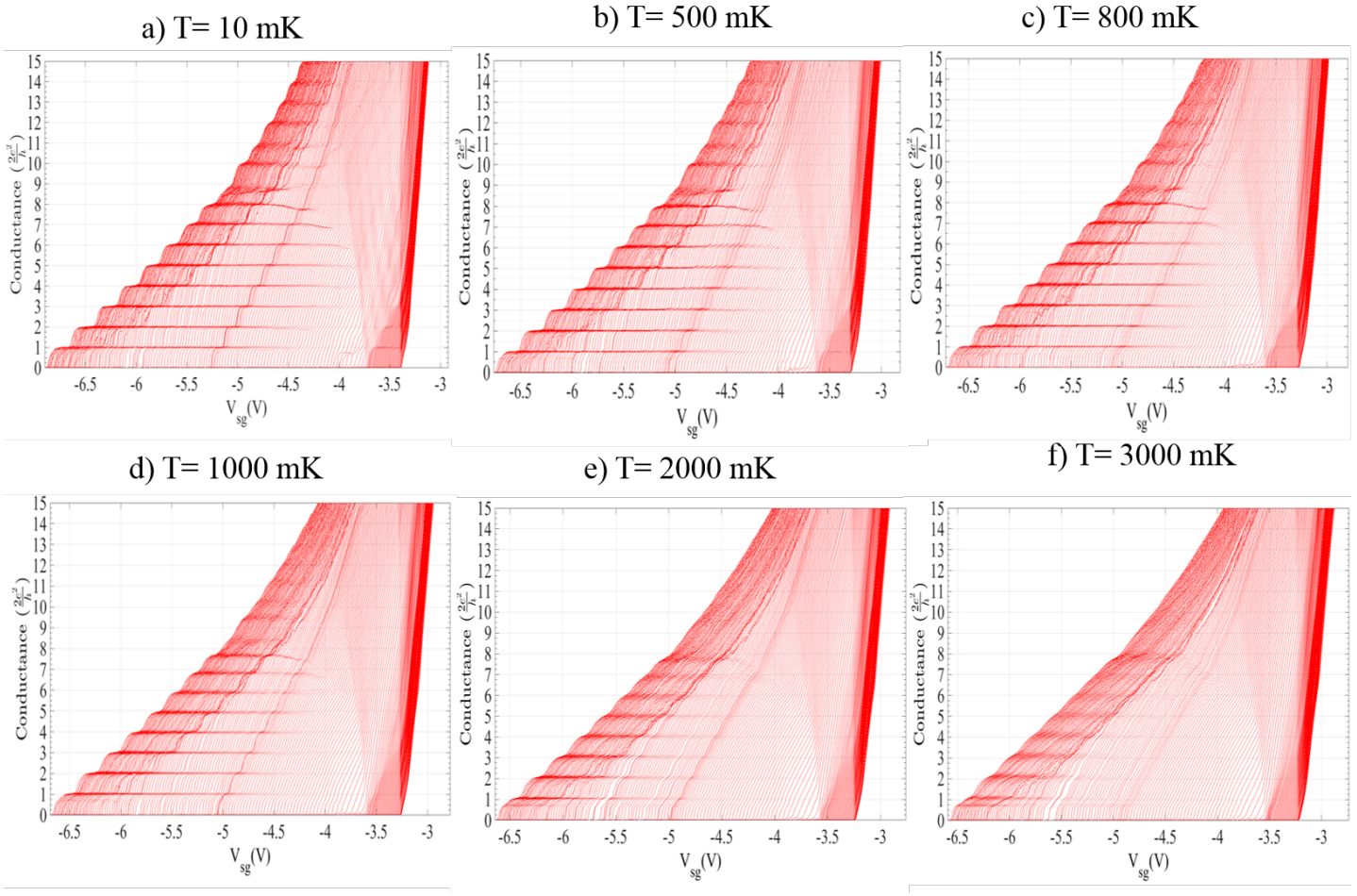

Figure 6.14: Conductance characteristics of the sample as the 1D channel is shifted laterally. The conductance is measured as a function of V_{mg} and V_{sg} is stepped from left-to-right in increments of -30 mV in all the plots. The temperature was varied from the base temperature of 10 mK to 3000 mK.

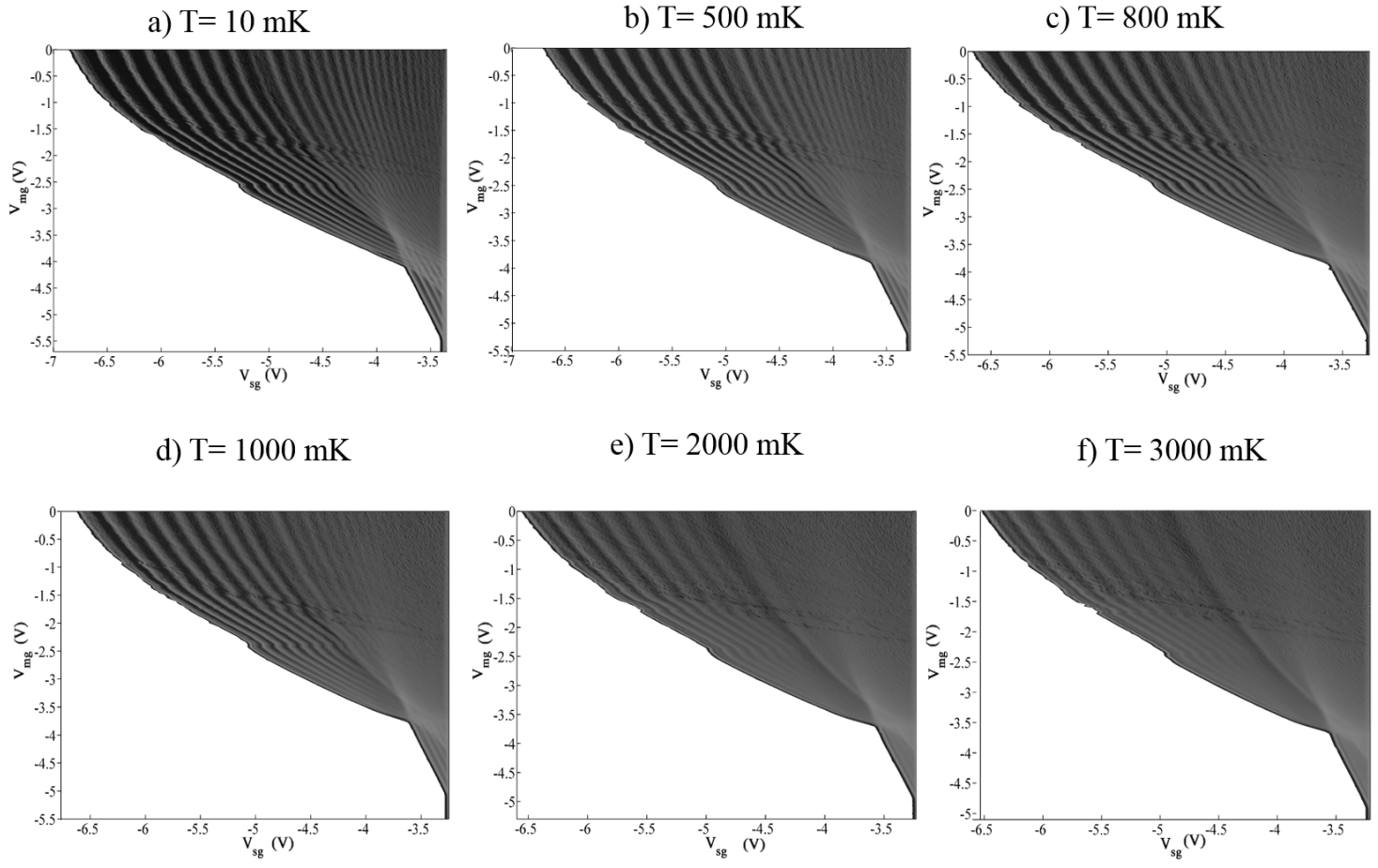

Figure 6.15: Greyscale plot of transconductance of the data in figure 6.14 ($\frac{dG}{dV_{sg}}$) as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

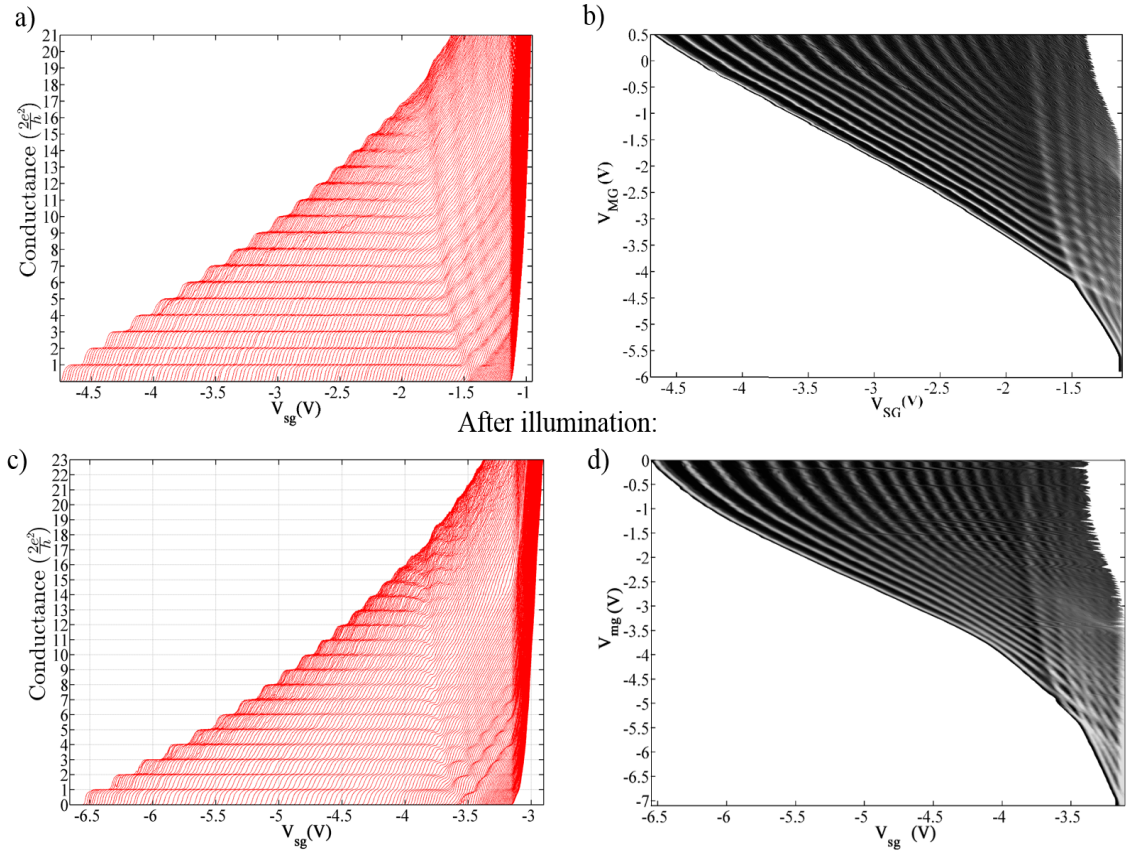

Figure 6.16: a) Conductance data from a mid-line gated device at T = 10 mK and electron temperature of $\sim$ 70 mK. For each trace V_{sg} is swept and V_{mg} is fixed. V_{sg} is incremented in steps -30 mV intervals from 0.0 V on the left to -5.9 V on the right. The split-gates have dimensions of 400 nm in length and 700 nm in width, with a 60 nm wide mid-line gate and c) after illumination using red LED. b) The greyscale $\frac{dG}{dV_{sg}}$ of figure 6.16 a) as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black while d) is the greyscale of figure 6.16 b) after illumination.

density of the 2DEG. Illuminating the sample using red LED increased the density, n_{2D}, to 4.0×10^{11} cm^{-2}. Figure 6.16 shows the conductance characteristics of the device before and after further illumination. Figure 6.16 c) shows that the plateaus at the mixing regime is much stronger after illumination compared to

figure 6.16 a) and the $\frac{4e^2}{h}$ plateau persists further in the mixing regime. Both the 1D wires also show significant changes. It may be noted that after the illumination the left and right 1D wires show very clear anticrossing of the ground and first excited states, respectively which was not evident in un-illuminated data shown in figure 6.16 (a and b). Also, comparing figure 6.16 b) and d), it is immediately obvious that the two 1D wires begin to couple. Further illumination enhances the coupling of the 1D wires and both 1D wires starts to anti-cross. This behaviour is entirely consistent with a phenomenon of increasing the density in the 1D wire as more electrons are available to couple through the mid-line gate.

6.6 Summary

In this chapter an experimental study of coupled 1D wires in a single 2DEG showing wavefunction-coupling of the two 1D wires using a 20 nm thin mid-line gate. The differential conductance measurements showed two 1D wires conducting as well as a mixing region in-between those wires. The mixing region shows complicated mixing of the subbands of the 1D wire where a clear crossing is observed. A temperature dependant study was performed to confirm that distinct regions are created by the mid-line gate are due to electrostatic confinement rather than electron interactions. The interaction effects between the two 1D wires can be tuned from crossing to anti-crossing by laterally shifting the 1D channel using asymmetric voltage. The dc-conductance measurements performed showed clear distinct regions of both 1D wires and their mixing regime each with different subband energy spacing. The dependence on density was investigated by controlled illumination of the device. The experimental results show that increasing the

density enhances the coupling of the 1D wires and both 1D wires starts to anti-cross. This behaviour is consistent with a phenomenon of increasing the density in the 1D wire as more electrons are available to couple through the mid-line gate.

Chapter 7

Interaction effects in back-gated quantum wires

7.1 Introduction

The interpretation of physical systems has been historically well understood in terms of free particle ensembles. The Hamiltonian of one such system is represented as the summation of N independent single particle Hamiltonians. In other words, the energy of the entire system is the sum of the energies of its constituent non-interacting particles. The fundamental units of all such systems are electrons. These electrons when confined spatially in less than two dimension may still be treated as non-interacting as long as their kinetic energy dominates the Coulomb interactions between them. However their individual characteristics weaken and exotic phases may start appearing when the Coulomb energy exceeds the kinetic energy. Such a one-dimensional (1D) system has been explained by the well-known Luttinger liquid (LL) model [129–131]. One of the simplest yet effective 1D systems is a quantum wire realised using a two dimensional electron gas (2DEG) in a GaAs/$A_xGa_{1-x}As$ heterostructure [15, 16, 42]. In a 1D quantum wire the conductance takes quantised values, with each 1D subband contributing a spin degenerate conductance of $2e^2/h$ and total conductance is $N(2e^2/h)$, where

$N = 1, 2, 3, 4$; here the non-interacting 1D electrons have freedom to change momentum in one dimension only with a progressive filling of the subbands. The ground state of such a system represents a true Fermi liquid exhibiting a conductance plateau at $2e^2/h$. However as the density of 1D electrons is reduced, their kinetic energy becomes comparable to the Coulomb energy which gives rise to various spin phases such as Winger lattice [18, 58, 61, 132], including recently observed splitting of single row of electrons into zig-zag and two rows [133]. In addition to this, when the electron-electron interaction is considered, a spin mode in addition to charge mode is predicted, which can't be explained in the framework of the general Luttinger Liquid model, as the electrons spin is incoherent in the low density regime [59, 134].

Despite their immense application for tuning the confinement in 1D quantum wires, the top gated split-gate devices have a limitation when a large negative voltage is applied on them which can screen the 2DEG underneath and any possible interaction effects [59]. Moreover, the fabrication of top gate requires two e-beam lithography stages, one for the split-gate and the other for the top gate [133]. Another alternative to realising 1D quantum wire with control over the confinement strength and interaction effects is to have a back gate on thinned semi-insulating GaAs wafer with sufficient separation from the 2DEG (50-100 μm). Also back gate fabrication does not require an additional e-beam stage and therefore this process is cost effective. A back gated, split-gate device has a unique advantage that is the field effect is weak, and the confinement can be tuned uniformly to investigate electron-electron interaction and hence spin-incoherent transport [135].

7.2 Experimental Methods

7.2.1 Wafer Details

The devices used in this chapter were fabricated on a delta doped GaAs/$Al_xGa_{1-x}As$ heterostructures. The two-dimensional electron gas is located 286 nm below the surface, with electron density, n_{2d}, $2.2 \times 10^{11} cm^{-2}$ and mobility μ of $7.95 \times 10^6 cm^2/Vs$ and further details of the wafer used, W731, is given in appendix A.

7.2.2 Measurement Setup

The measurements presented in this chapter were performed in a cryogen-free dilution refrigerator with a base temperature of 10 mK and electron temperature of $\sim$ 70 mK. Two terminal differential conductance $G = \frac{dI}{dV}$ was measured with a sinusoidal excitation voltage of 10 μV at frequency of 77 Hz. The dependant magnetic-field measurements were conducted with magnetic field orientations of in-plane and perpendicular to the 2DEG.

7.2.3 Device Fabrication

The quantum wire is defined using a pair of split-gate on the top of the GaAs/$A_xGa_{1-x}As$ heterostructure and a specially designed Schottky back gate has been used to tune the density of the 1D electrons. Split-gates devices were drawn using electron-beam lithography and Ti/Au was deposited to form the Schottky gates. Six split-gate devices with a length of 400 nm and width of 500 nm with different split-gate profile were measured and all showed typical 1D behaviour. For back gate fabrication, firstly, the wafer had to be thinned down from 550 μm to 100-

50 μm to effectively reduce the requirement to apply a large negative voltage to modulate the density of electrons in the 2DEG and for, more details of the fabrication techniques of the back gate can be found in chapter 4. Figure 7.1 shows a scanning electron microscopy images of a comparison between un-etched (550 μm thick chip) and etched chip (50 μm thick) with a back gate. Figure 7.2 shows the schematic diagram of the back gated, split-gate device fabricated on a GaAs/A_xGa_{1-x}As heterostructure.

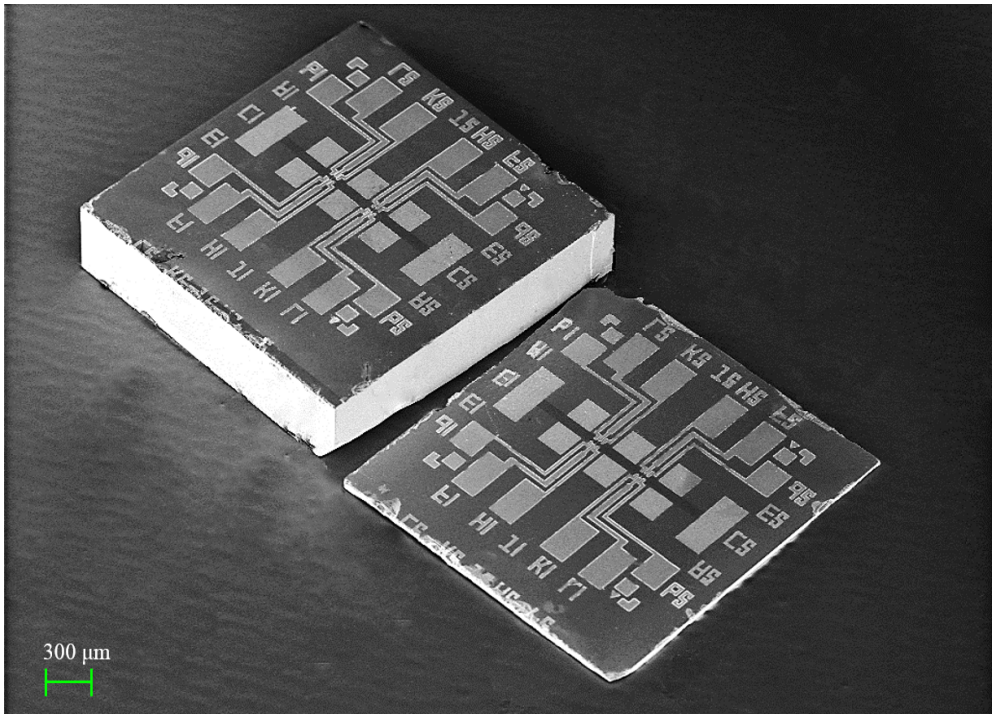

Figure 7.1: Scanning electron microscopy images of the fabricated as well as etched GaAs chips. The figure shows a chip before etching (top) with a thickness of 550 μm and after etching to a thickness of 50 μm (bottom).

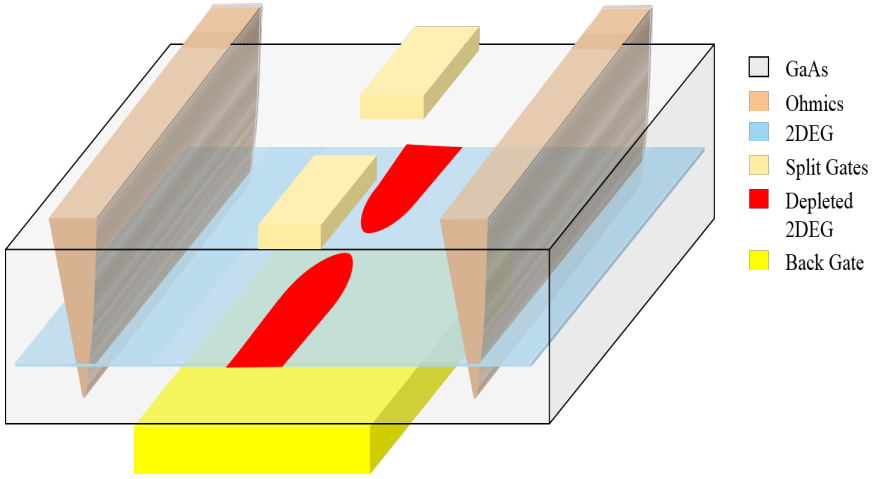

Figure 7.2: A schematic diagram of the 1D device showing a pair of split-gate, Ohmics contacts for source and drain, a back gate for tuning the carrier density in 1D quantum wire.

7.3 Results

Split-gate devices with a back gate were used for performing the measurements. The split-gate device has a length of 400 nm and width of 500 nm and the devices were fabricated on a delta doped GaAs/$Al_xGa_{1-x}As$ heterostructures and further details of the wafer used, W731, is given in appendix A and back gate fabrication details have been given in chapter 4. This section addresses a more comprehensive study of the interactions effects in back gated 1D quantum wires.

7.3.1 Back Gate Characteristics

Figure 7.3 shows the reverse and forward sweeps of the differential conductance of the 2DEG as a function of the voltage applied to the back gate without any bias applied to the split-gate. The traces show the effect of the back gate voltage on the conductance of the 2DEG. As the back gate is made more negative

the conductance drops and the channel gets fully pinched-off at V_{bg} $\sim$ -120 V. This indicates that back gate can achieve a wide range of electron density. It may be noted that there is hardly any significant hysteresis between the forward and backward traces indicating a good quality of fabricated back gate device. The 2DEG density of electrons, n_{2D}, was estimated to be $1.2 \times 10^{11} cm^{-2}$ using conventional Shubnikov-de Haas (SdH) oscillations. Another method was used to estimate n_{2D} using the back gate voltage required to deplete the 2D electrons in two terminal conductance measurement when the split-gate were held at zero voltage. At V_{bg}= -120 V, the channel was completely pinched off, therefore using V_P= -120 V in the relation $V_P = en_{2D}D/\epsilon\epsilon_0$, where e is charge of electron, n_{2D} is 2DEG density, D is the distance of back gate from the 2DEG (50 μm), ϵ is dielectric constant of GaAs (12.5), and ϵ_0 is permittivity of free space, the n_{2D} $\sim 1.73 \times 10^{11} cm^{-2}$ which is in close approximation to the value estimated using SdH oscillations.

7.3.2 Confinement potential Control

Figure 7.4 shows the conductance traces as the split-gate voltage is swept for various back gate voltages. The back gate voltage for the left most trace is 0 V which is incremented by -2 V so that the right most trace is taken for V_{bg} $\sim$ -120 V. Following the conductance traces from left to right the confinement potential is changing from a strongly-confined regime to a weakly-confined regime. Moving from weak-to-strong confinement, the plateaus become longer and well defined which indicates increasing subband spacing. As the back gate voltage is made more negative, the pinch-off voltage of the split-gate, V_{sg}, moves to

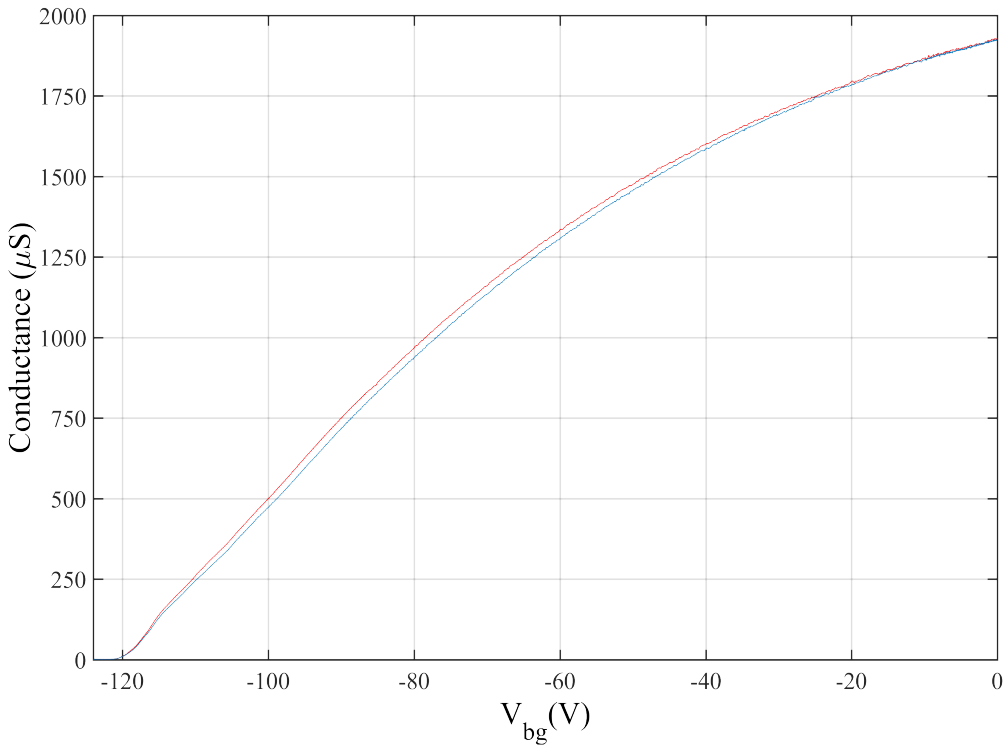

Figure 7.3: The differential conductance measurements of 2DEG by sweeping the back gate without any voltage on the split-gate. The conductance decreases as the back gate is made negative till the channel is fully pinched off at -120 V.

lower negative voltages which indicates a lower carrier density. It is important to note that the back gate voltage controls the density of electrons not only in the vicinity between the split-gate but for the entire 2DEG. Therefore, the series resistance was removed individually for each traces in figure 7.4 and in other figures in this chapter where the series resistances was 370 Ω for V_{bg} = 0 and 3700 Ω for V_{bg} = -120 V and the series resistance values were chosen such that the conductance plateaus aligns best to their known quantised values. It may be

noted however that as the 1D behaviour moves to the weaker confinement regime the 0.7 structure was found to strengthen.

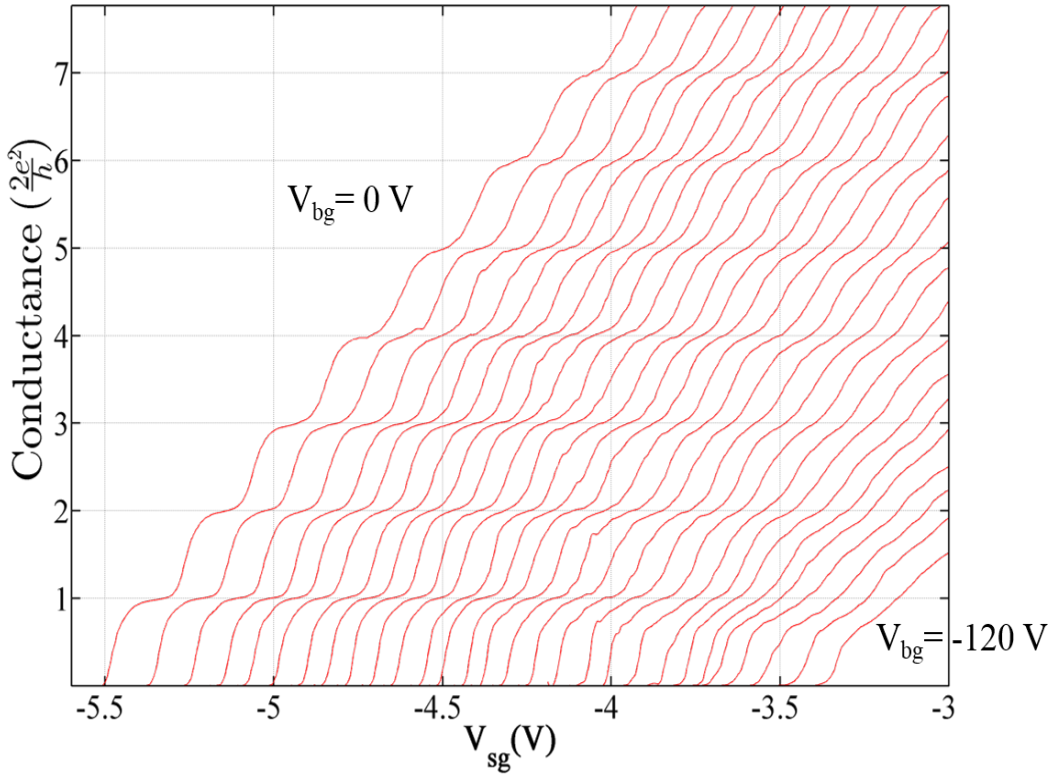

Figure 7.4: Conductance data from a back gated device at T = 10 mK and electron temperature of $\sim$ 70 mK. For each trace V_{sg} is swept and the back gate voltage, V_{bg}, is fixed. V_{bg} is incremented in steps -2 V intervals from 0 V on the left to -120.0 V on the right. The split-gate have dimensions of 400 nm in length and 500 nm in width.

Figure 7.5 shows the greyscale plot of data, shown in figure 7.4. The plateau weakens with weakening the confinement, moreover, the 0.7 was found to strengthen when the confinement was weak (figures 7.4 and 7.5).

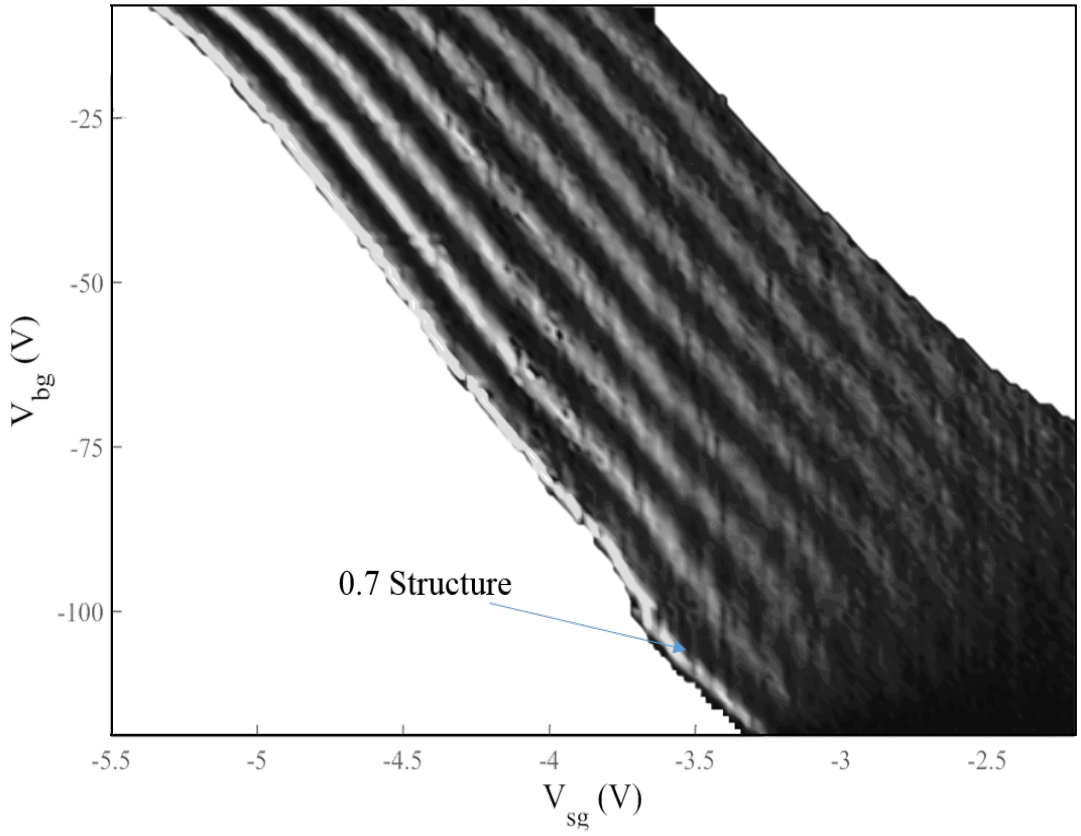

Figure 7.5: Greyscale plot of transconductance of the data in figure 7.4, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{bg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

7.3.3 Perpendicular Magnetic Field

The section describes the effect of applying a perpendicular magnetic field on the conductance traces as the back gate voltage is varied. The rectangular split-gate used in this section has dimensions of 400 nm in length and 500 nm in width. Figure 7.6 shows that the application of a perpendicular magnetic field widens the sub-band spacing compared to the situation with no magnetic field. The application of perpendicular magnetic field changes the conductance plateaus as

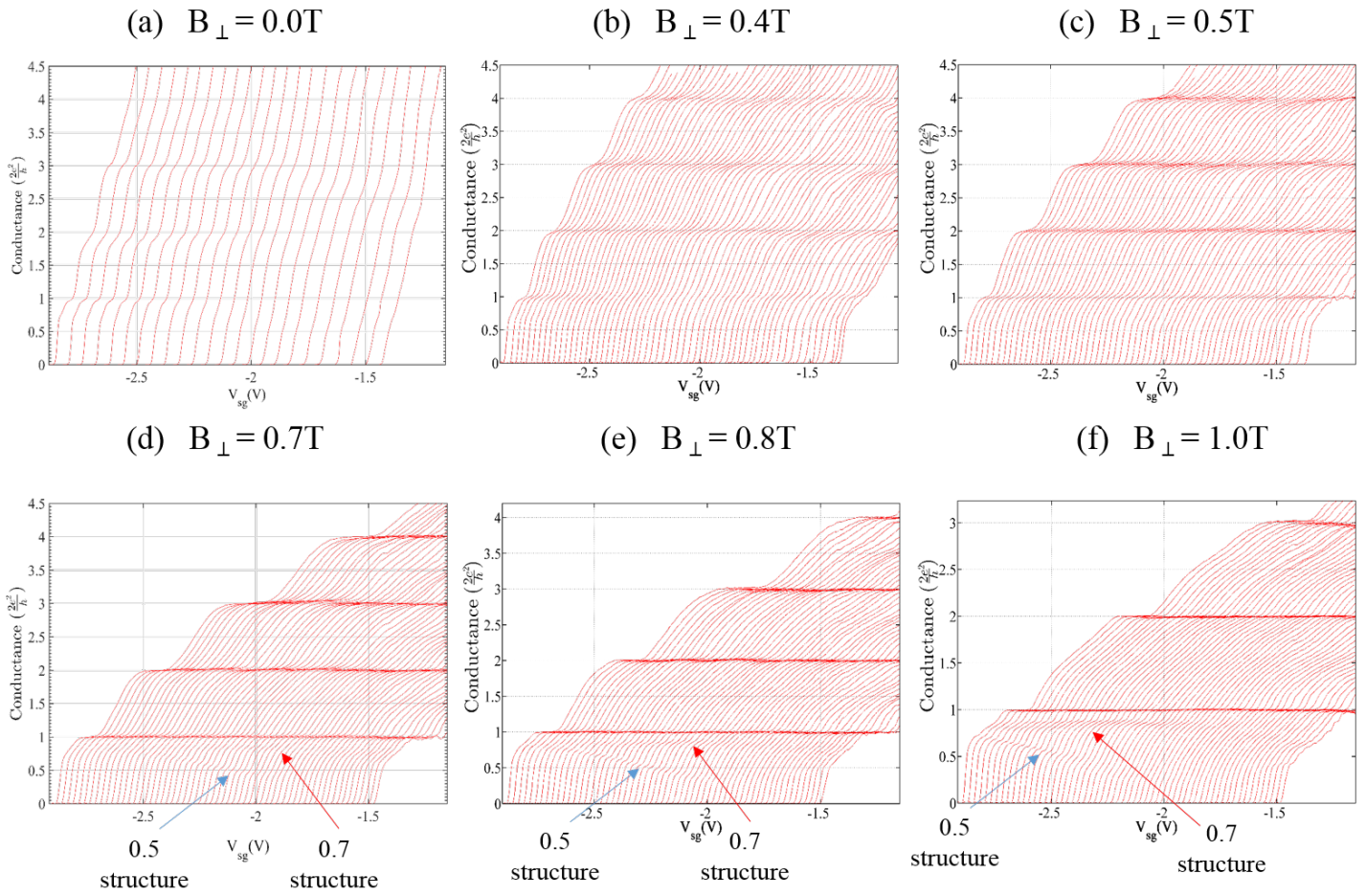

Figure 7.6: Conductance characteristics of the split-gate device as a perpendicular magnetic field is increased from 0.0 T to 1.0 T. In a), the conductance is measured as a function of V_{sg}, and V_{bg} is stepped from -0.0 V on the left to -120 V on the right, in intervals of -5 V. In b) to f) V_{bg} is stepped from 0.0 V on the left to -120 V on the right in intervals of -1 V. In b) 0.7 structure is seen in the weaker confinement regime.

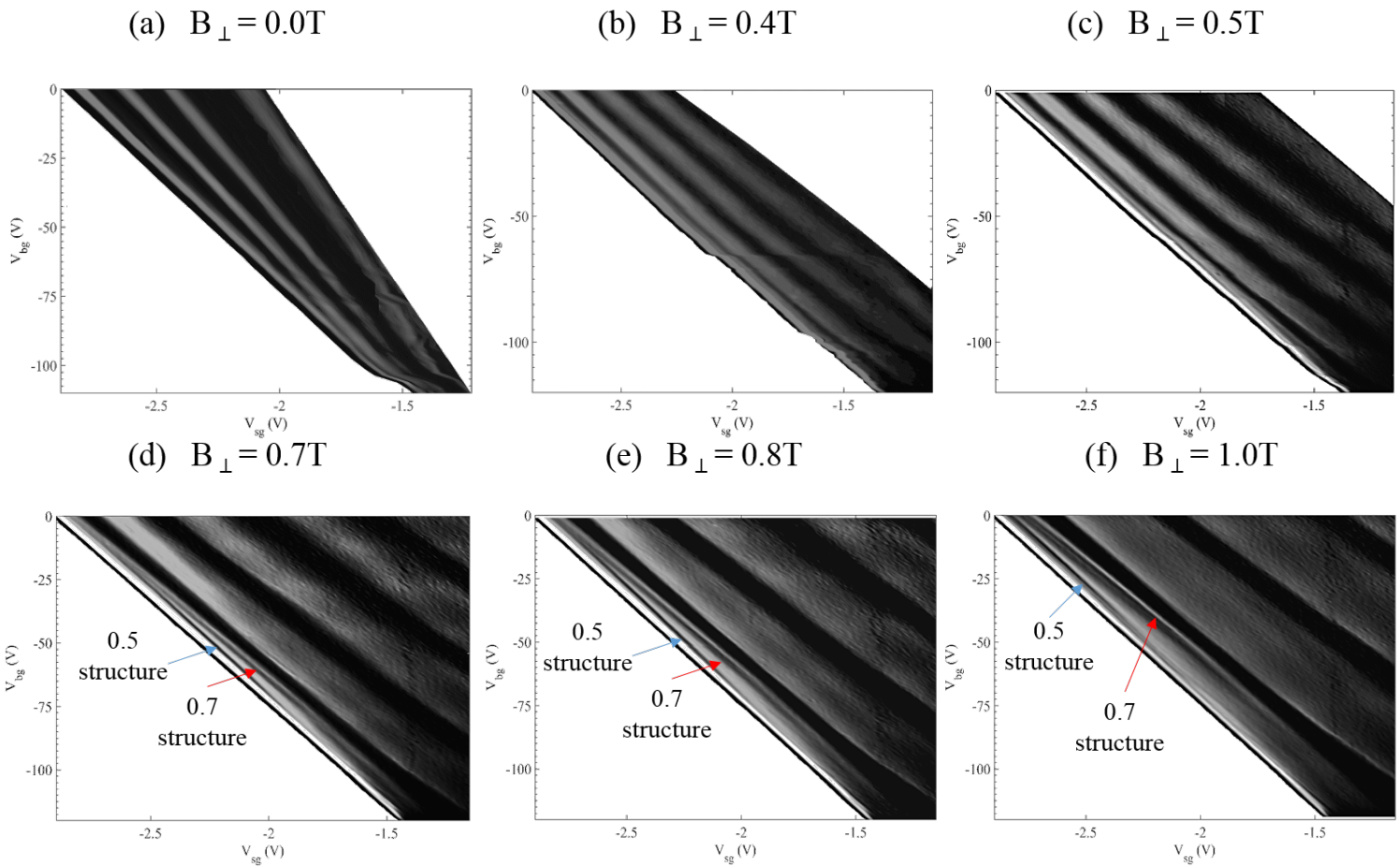

Figure 7.7: Greyscale plot of transconductance of the data in figure 5.6, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{mg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

they increase in length, across the whole range of confinement. This reflects an increase in subband spacing due to the additional confinement from the magnetic field and subsequent magnetic depopulation of higher 1D subbands. The conductance and the quality of the quantisation should improve and be cleaner in the presence of a perpendicular magnetic field due to the reduction in backscattering. Figure 7.7 shows the greyscale plots of figure 7.6 in different perpendicular magnetic fields varied from 0.0 T to 1.0 T. As the magnetic field is increased the subband spacing increases and magneto-electric depopulation of higher subbands occurs.

Figure 7.7 a) shows the first three subbands in the units of $2e^2/h$ in the absence of a perpendicular magnetic field. The 0.7 structure is always seen in the strong confinement when the perpendicular magnetic field is varied from 0.0 T to 1.0 T. Figure 7.7 b) shows that in the strong confinement regime, regular plateaus in the units of $2e^2/h$ are observed and an additional structure at 0.7 is also seen in figure 7.6. It was found that the 0.7 strengthened, weakened and strengthened again as the confinement was gradually weakened by making the back gate more and more negative.

On further increasing the magnetic confinement by increasing the perpendicular magnetic field to 0.5 T (see figure 7.6 c), and figure 7.7 c)), the 0.7 structure in the strong confinement drops down to around 0.5 as the confinement is weakened and at about $V_{bg} \sim$ -75 V, a structure at 0.7 reappears and strengthens on further weakening the confinement.

On further increasing the magnetic confinement by increasing the perpendicular magnetic field to 0.7 T (see figure 7.6 d), and figure 7.7 d)). As the confinement is weakened and at about $V_{bg} \sim$ -35 V, a new (second) structure at

0.5 appears along with the 0.7 structure which strengthens on further weakening the confinement. In the weak confinement regime at $V_{bg} \sim$ -100 V, the structure at 0.5 disappears and 0.7 structure strengthens.

Increasing the magnetic confinement further by increasing the perpendicular magnetic field to 0.8 T (see figure 7.6 e), and figure 7.7 e)). As the confinement is weakened in the intermediate confinement regime, a structure at 0.5 appears along with the 0.7 structure. The 0.7 structure then weakens and eventually evolves to 0.5 in the weak confinement regime at $V_{bg} \sim$ -100 V.

Increasing the perpendicular magnetic field to 1.0 T (see figure 7.6 f), and figure 7.7 f)). As the confinement is weakened, the 0.7 structure is seen alongside 0.5 structure. The structure at 0.5 then disappears on further weakening the confinement and in the intermediate confinement regime, only 0.7 structure appears. In the weak confinement regime, a structure at 0.5 appears alongside 0.7 at $V_{bg} \sim$ -110 V.

From the results, it appears that the 0.7 and 0.5 are co-related and the origin of one appears to be related to the other. Also, as we reduced the density and weakened the confinement the weakening and strengthening of 0.7 or 0.5 and gradually moving of 0.7 into 0.5 suggests that they are related and could be due to intrinsic spin polarisation of the 1D system. It may be noted that the dynamics of 0.5/0.7/0.5 is seen in the low density regime therefore their origin could be related to exchange but we have no direct evidence to prove it at this stage. These results were obtained with a perpendicular magnetic field. In the next section, the back gating effect in the absence of perpendicular field is predicted to show spontaneous spin polarisation is presented. The next section is based on pointed split-gate with length of 500 nm and width of 400 nm.

7.4 Possible Spin polarisation in Quantum Wires

Berggen *et al.* predicated that the spin polarisation of 1D subbands can occur even in the absence of a large magnetic field in the lower subbands at low electron densities [62]. The calculations were done at B = 0.01 T for an infinitely long quantum wire in the presence of in-plane magnetic field. At low densities, the 1D wire can be fully spin polarised and the first conductance plateau is expected at $0.5(2e^2/h)$. When spin polarisation occurs as the density is decreased by sweeping the gates, the effective transmission barrier becomes different for the two spin directions [63]. When spin polarisation occurs at low densities, the conductance should be equal to or larger than $0.5(2e^2/h)$ but the exact value may be device dependent. The spin splitting is caused by the exchange potential and not by the Zeeman splitting. Berggen *et al.* have done further calculations using a finite-length 1D quantum wire instead and also the potential was modelled as a saddle-point and it confirmed that spin polarisation occurs as the electron density is lowered and thus the effective barrier height is different for spin up and spin electrons [63, 64].

7.4.1 Results

Split-gate used in this section has dimensions of 400 nm in width and 500 nm in length and has pointed profile. The pointed profile of the pair of split-gate are two rectangular corners offset at 45 degrees and have radius of curvature of around 20 nm. Figure 7.8 shows the differential conductance plot when the split-gate voltage, V_{sg}, was swept for various back gate voltages, V_{bg}, from 0 V (left, the strong confinement) to -32 V (right, the weak confinement) in steps of -1 V. The

confinement is weakened by increasing the back gate voltage and this reduces the carrier density . When V_{bg} is zero, quantised plateaus occur at multiples of $2e^2/h$ and in addition, a structure at 0.7 is seen. On further increasing the back gate voltage and making the confinement further weaker at V_{bg}= - 20 V, the structure at $0.5(2e^2/h)$ alongside the ground state at $2e^2/h$ is observed and the structure at $0.5(2e^2/h)$ strengthens further as the carrier density is further reduced and reduces below $0.5(2e^2/h)$. This a signature of a spin polarised 1D electrons that only manifests in low electron density regime. Figure 7.10 shows the greyscale plot of data, shown in figure 7.8. The first three subbands are clearly seen in figure 7.10 and at back gate voltage beyond -20 V, there is a clear splitting of the ground state to branches indicating spin up and spin down and this splitting has been indicated by a blue line. The evolution of the inflection point where the 0.7 structure occurs was tracked as the back gate, V_{bg}, was made progressively negative and is shown in figure 7.9. It can be seen that the 0.7 structure evolves to 0.5 structure and stays there before settling below $0.5(2e^2/h)$ as the V_{bg} is more negative.

7.5 Spin-Incoherent Transport

Spin-incoherent transport has re-gained interest due to recent experimental and theoretical works on such systems [25, 59, 134]. A spin-incoherent LL is characterised by the fact that if the temperature is higher than the characteristic spin scale and less than Fermi energy, spin becomes totally incoherent at a finite temperature while charge remains close to its ground state [60]. Such a system has distinction of having spin modes as well, therefore the conductance measurement

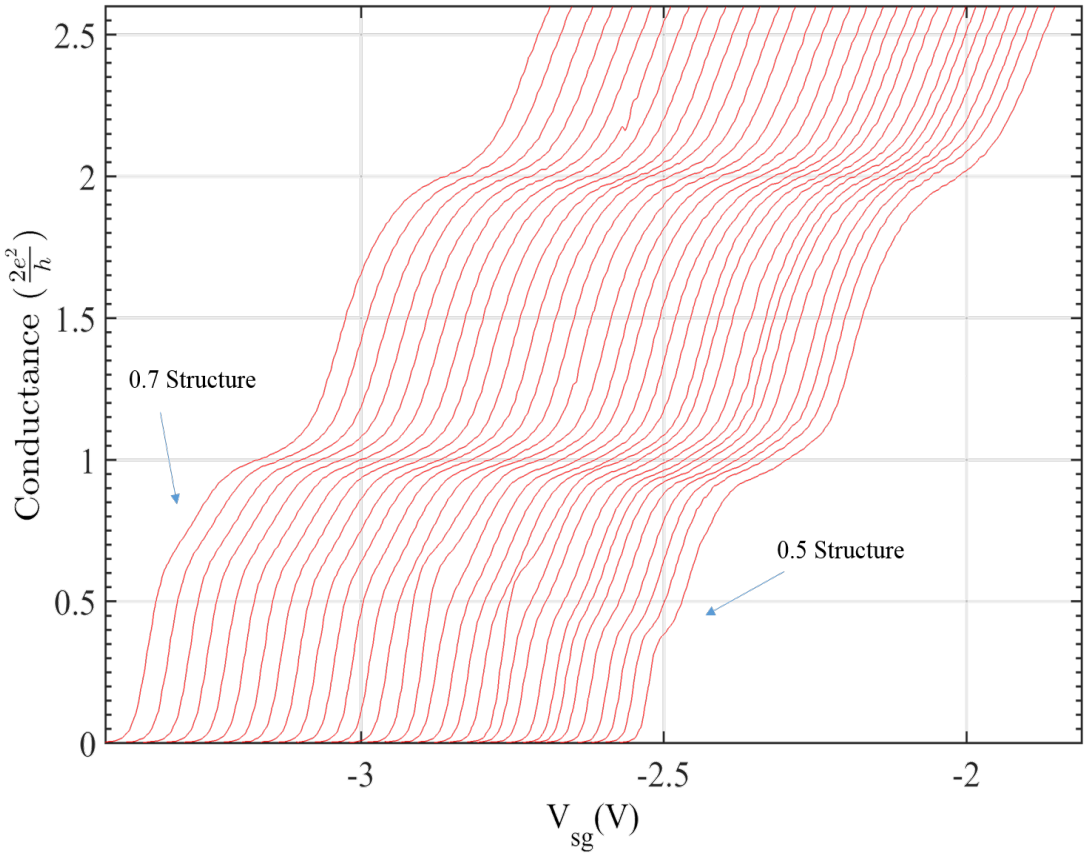

Figure 7.8: The differential conductance measurements of a split-gate device with a back gate. For each trace, the conductance is measured as a function of split-gate voltage ,V_{sg}, at a fixed value of back gate voltage, V_{bg}. V_{bg} is incremented in steps of -1 V from 0 V on the left to -32 V on the right. The conductance traces from left to right means that the confinement of 1D wire is changing from strong to weak depending on the applied back gate voltage. The ground state plateau occurs at $2e^2/h$ and as the density of 1D electrons is reduced and in the weaker confinement, a structure at $0.5(2e^2/h)$ starts appearing alongside the ground state which strengthens when the carrier density is further reduced.

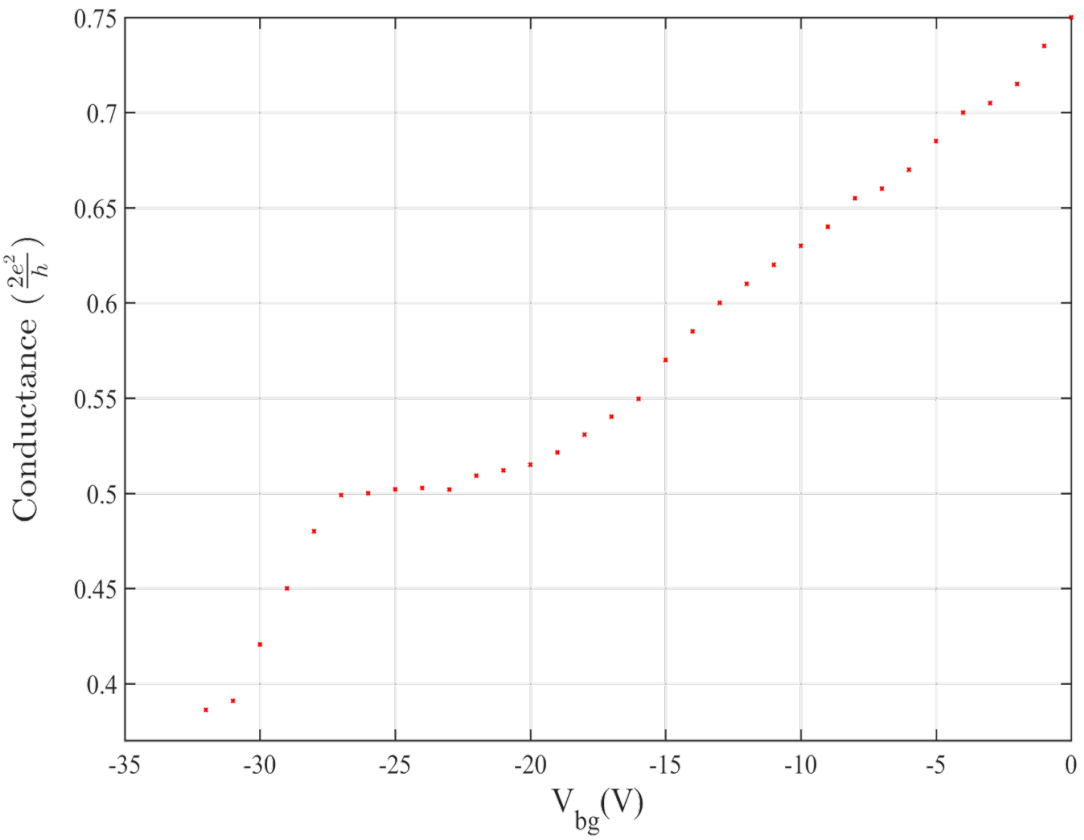

Figure 7.9: A graph showing the position of the inflection point of the 0.7 structure in units of $2e^2/h$ and its evolution versus V_{bg}. V_{bg} is incremented in steps of -1.0 V from 0 V on the left to -32 V on the right.

shows plateau at e^2/h rather than the usual $2e^2/h$ [59, 61]. Previously, spin-incoherent transport was studied in top gated, split-gate devices on a modulation doped GaAs/A_xGa_{1-x}As heterostructure [19].

7.5.1 Results

The section describes the effect of in-plane magnetic field on the conductance of a weakly confinement longer 1D wire. The split-gate in this section are pointed

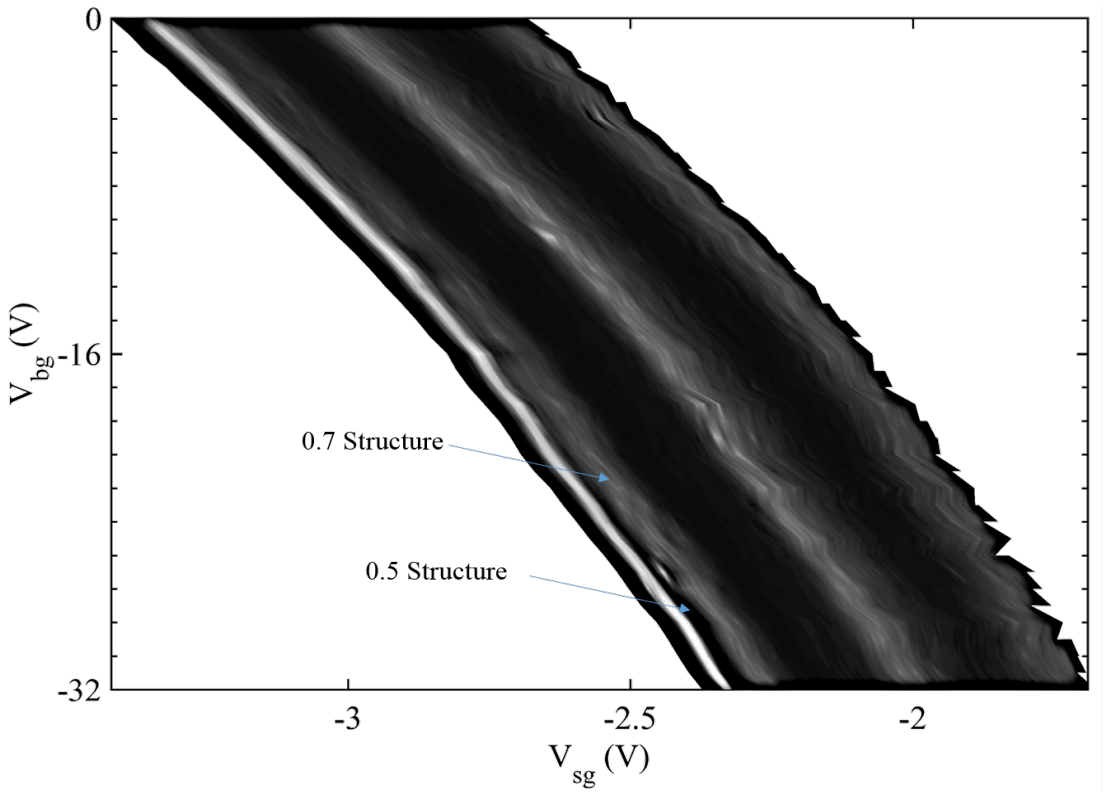

Figure 7.10: Greyscale plot of transconductance of the data in figure 7.8, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{bg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

split-gate with dimensions of 400 nm in width and 500 nm in length and a back gate voltage of -225 V was required to pinch off the channel.

Figure 7.11 shows the differential conductance plot when the split-gate voltage, V_{sg}, was swept for various back gate voltages, V_{bg}, from 0 V (left, the strong confinement) to -225 V (right, the weak confinement) in steps of -5 V. Figure 7.11 shows the first four plateaus in multiples of $2e^2/h$ and as the confinement was weakened by increasing the back gate voltage, the higher conductance plateaus starts getting weaker. On further increasing the back gate voltage and making

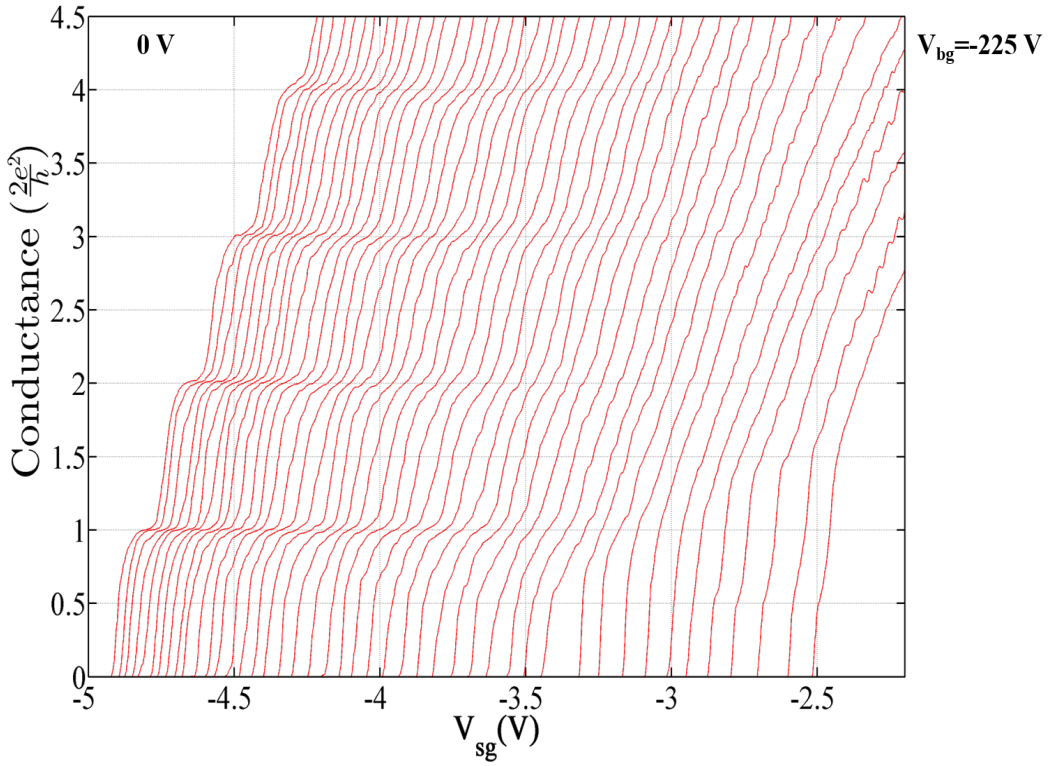

Figure 7.11: The differential conductance measurements of a split-gate device with a back gate. For each trace, the conductance is measured as a function of split-gate voltage ,V_{sg}, at a fixed value of back gate voltage, V_{bg}. V_{bg} is incremented in steps of -5 V from 0 V on the left to -225 V on the right. The conductance traces from left to right means that the confinement of the 1D wire is changing from strong to weak depending on the applied back gate voltage. The plateaus become shorter and less defined as the confinement (and the density of 1D electrons) is reduced and in the weaker confinement, a structure at $0.5(2e^2/h)$ starts appearing which strengthens at V_{bg} = -225 V when the carrier density is further reduced.

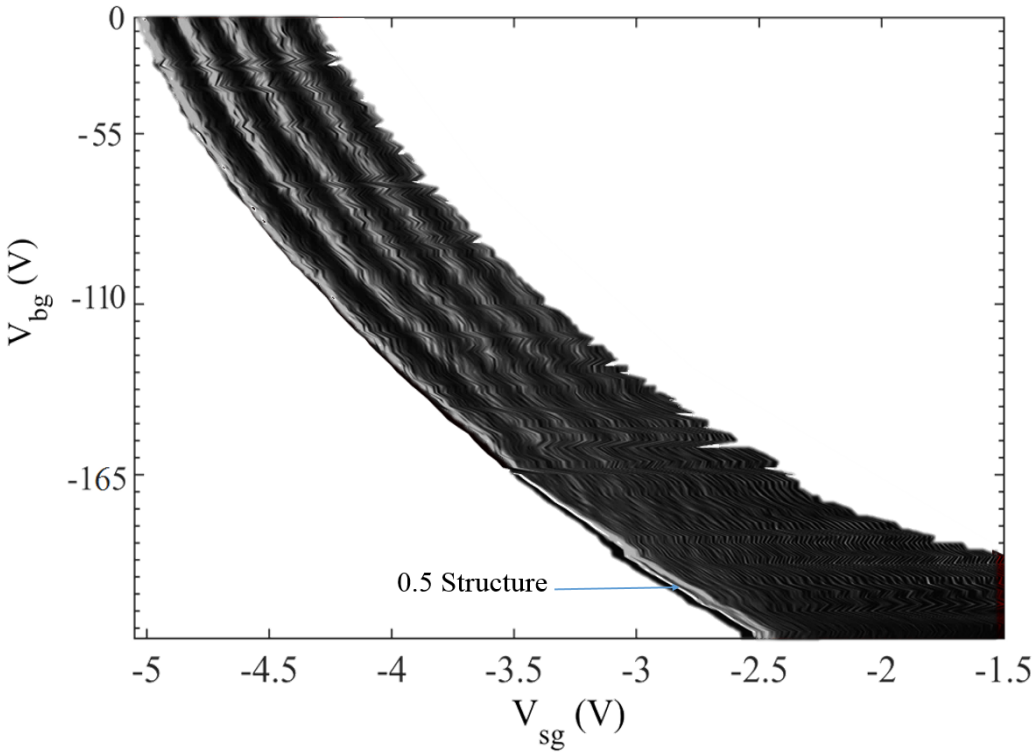

Figure 7.12: Greyscale plot of transconductance of the data in figure 7.11, $\frac{dG}{dV_{sg}}$, as a function of V_{sg} and V_{bg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

the confinement further weaker at V_{bg}= -225 V a structure at $0.5(2e^2/h)$ was observed without any signature of $2e^2/h$. Figure 7.14 shows the greyscale plot of data, shown in figure 7.13. The first four subbands are clearly seen in figure 7.12 and at back gate voltage beyond -200 V, there is a clear structure at $0.5(2e^2/h)$ with the disappearance of the ground state. Figure 7.13 shows the conductance plot in the presence of in-plane magnetic field of 12 T, the field direction is parallel to the current direction in the 1D quantum wire. This measurement was performed in a different cool down therefore the split-gate voltages are different

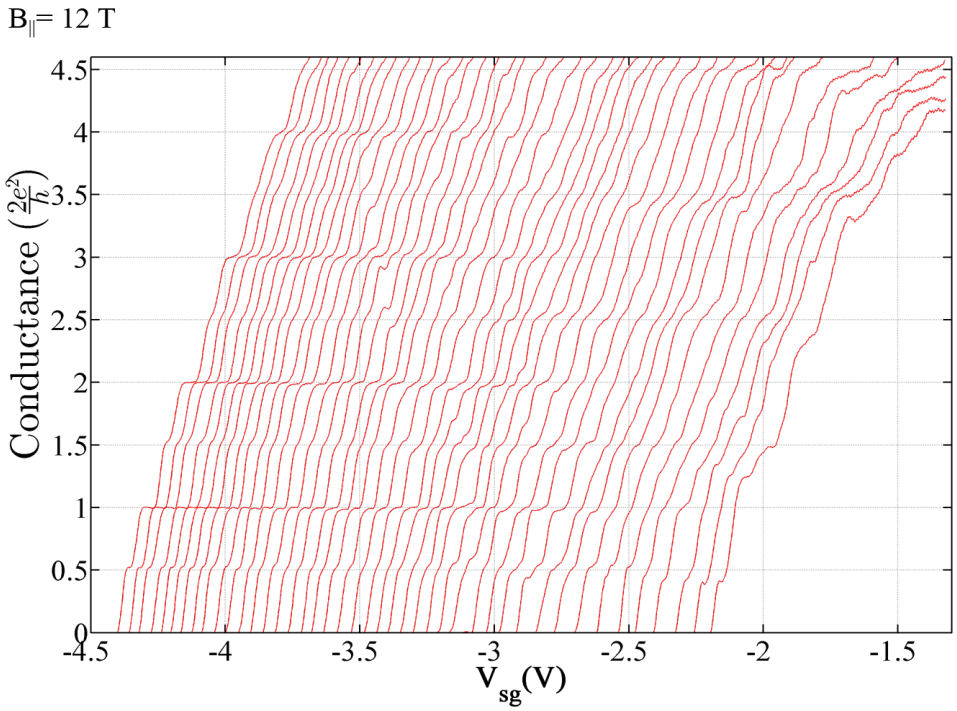

Figure 7.13: The differential conductance measurements of a split-gate device with a back gate in the presence of 10 T in-plane magnetic field. For each trace, the conductance is measured as a function of split-gate voltage ,V_{sg}, at a fixed value of back gate voltage, V_{bg}. V_{bg} is incremented in steps of -5 V from 0 V on the left to -225 V on the right. The conductance traces from left to right means that the confinement of 1D wire is changing from strong to weak depending on the applied back gate voltage. There is clear spin splitting of the quantised plateaus and the appearance of half-integer plateaus.

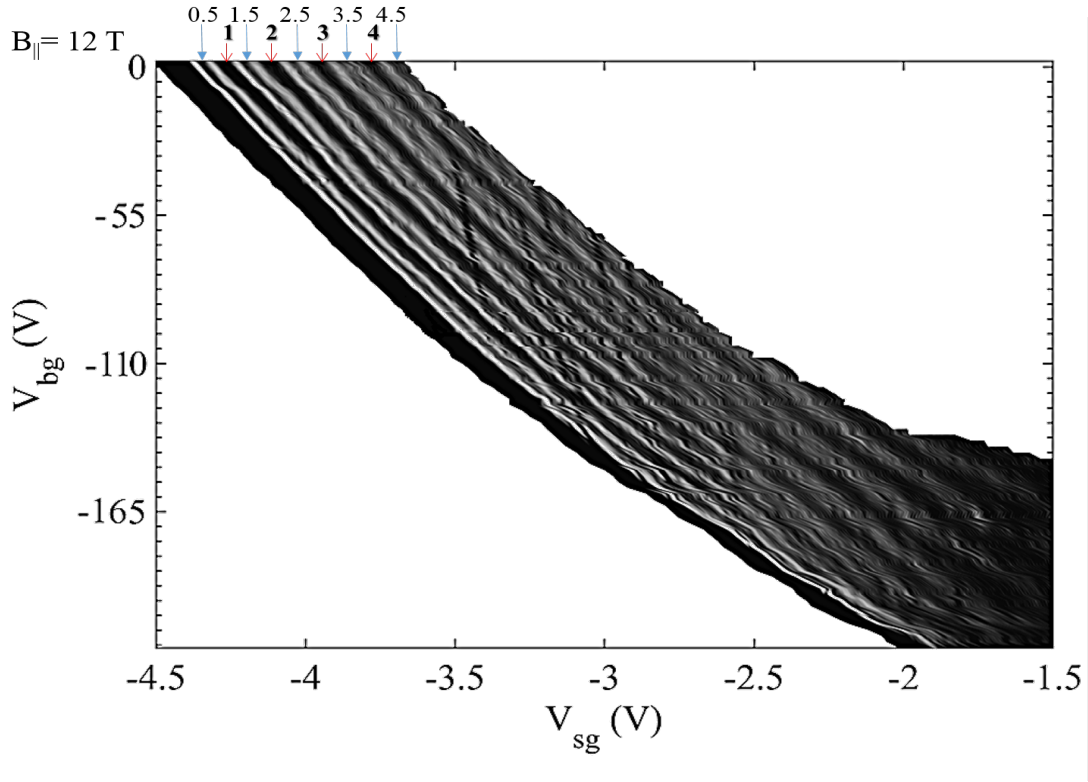

Figure 7.14: Greyscale plot of transconductance of the data in figure 7.13, $\frac{dG}{dV_{sg}}$, in the presence of 12 T in-plane magnetic field as a function of V_{sg} and V_{bg}. Regions of high transconductance are shown in grey and low transconductance (plateaus) in black.

in figure 7.13 and figure 7.11. Figure 7.13 shows the appearance of half-integer plateaus at $0.5(2e^2/h)$ due to Zeeman splitting of 1D subbands alongside integer plateaus which are multiples of $2e^2/h$ and can be seen clearly in the greyscale plot in figure 7.14.

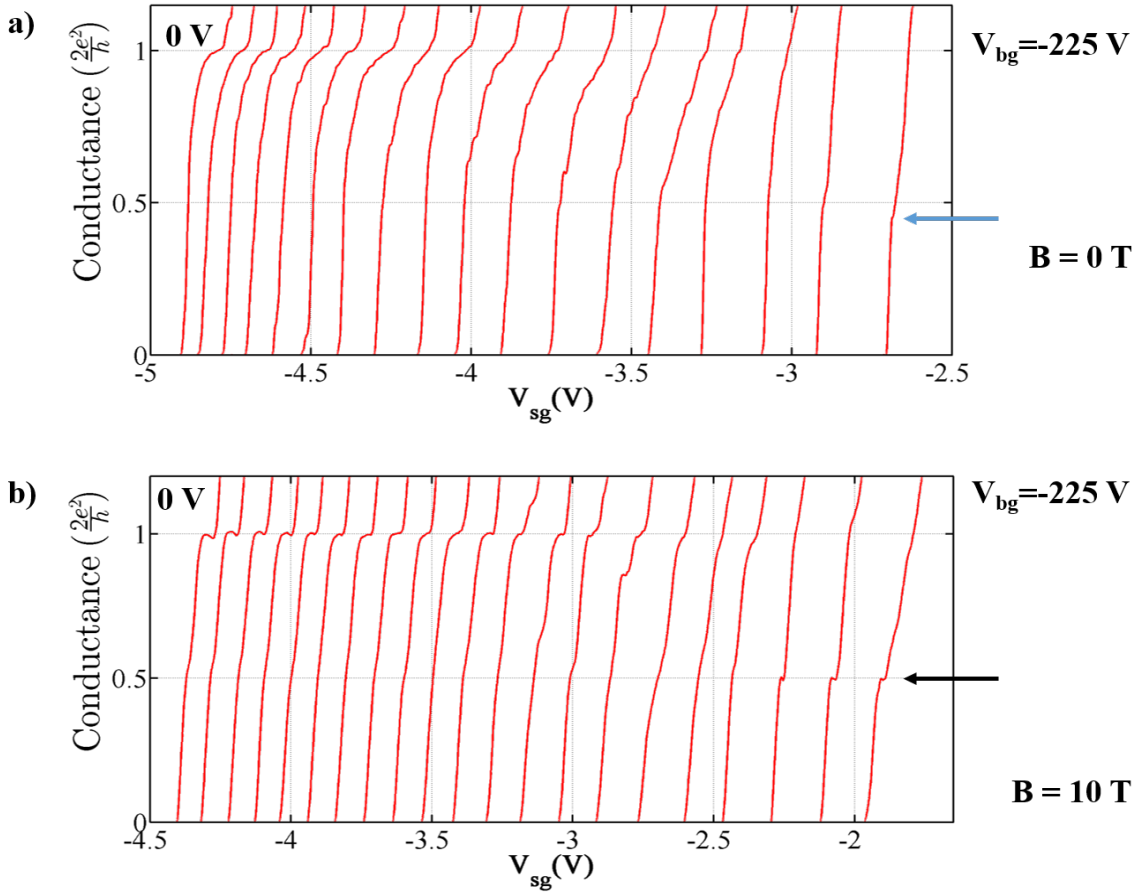

Figure 7.15: The differential conductance measurements of a split-gate device with a back gate; for comparison, data in the presence of in-plane magnetic field of 10 T are also shown. For each trace, the conductance is measured as a function of split-gate voltage (V_{sg}) at a fixed value of back gate voltage, V_{bg}. V_{bg} is incremented in steps of -12.5 V from 0 V on the left to -225 V on the right. The conductance traces from left to right means that the confinement of 1D wire is changing from strong to weak depending on the applied back gate voltage. a) The ground state plateau represented by $2e^2/h$ becomes shorter and less defined as the confinement (and the density of 1D electrons) is reduced and in the weaker confinement, a structure at e^2/h starts building up which strengthens at V_{bg} = -225 V when the carrier density is further reduced as indicated by a blue arrow, b) conductance plots in the presence of in-plane magnetic field of 10 T. The usual spin polarised conductance plateau at e^2/h was observed in the strong confinement which strengthened in the weaker confinement indicated its spin-incoherent origin (indicated by a black arrow).

7.5.2 Discussion

Figure 7.15 shows the differential conductance plot when the split-gate voltage, V_{sg}, was swept for various back gate voltages, V_{bg}, from 0 V (left, the strong confinement) to -225 V (right, the weak confinement) in steps of -12.5 V. It may be noted from Figure 7.15 (a) that as the confinement was weakened by increasing the back gate voltage, the first conductance plateau appearing at $2e^2/h$ starts getting weaker with the appearance of the $0.7(2e^2/h)$ structure. On further increasing the back gate voltage and making the confinement further weaker at V_{bg}= -225 V a structure at $0.5(2e^2/h)$ was observed without any signature appearing at $2e^2/h$ (shown by a black arrow). Figure 7.15 (b) shows the conductance plot in the presence of in-plane magnetic field of 10 T, the field direction is parallel to the current direction in the 1D quantum wire. This measurement was performed in a different cool down therefore the split-gate voltages are different in (a) and (b) plots.

On application of large in-plane magnetic field the conductance plateau, e^2/h which appeared at V_{bg}= -225 V in the absence of magnetic field in (a) gets strengthened as indicated by a black arrow in (b). In general, application of a large in-plane magnetic field lifts the spin degeneracy and half integer plateaus start getting resolved. Looking at the strong confinement regime on the right of the plot in (b), it may be seen the appearance of half integer plateau $0.5(2e^2/h)$ in addition to $2e^2/h$, due to Zeeman splitting of 1D subbands [133]. As the confinement was weakened, like the case in (a), the $2e^2/h$ gets weaker and weaker with increasing back gate voltage and eventually disappears at V_{bg}= -225 V. The $0.5(2e^2/h)$ shows a very interesting behaviour as we tuned the confinement, i.e.,

$0.5(2e^2/h)$ in the strong confinement first weakens and then strengthens as the confinement was weakened as indicated by vertical down-arrows in (b), however in the very low density regime in the weakest confinement regime the $0.5(2e^2/h)$ strengthens again, as indicated by a horizontal arrow on the right side of (b).

7.5.2.1 Transconductance Characteristics

A better picture of the scenario can be seen when we plot transconductance, dG/dV_{sg} as a function of split-gate voltage. Figure 7.16 shows the numerical dG/dV_{sg} of the data shown in figure 7.15. As before, figure 7.16 (a) is the measurement performed in the absence of magnetic field and figure 7.16 (b) shows the measurement performed in the presence of in-plan magnetic field of 10 T. Traces have been offset vertically for clarity. The top traces in both the plots were taken at V_{bg}= 0 V and successive traces have been taken when the back gate was incremented by -12.5 V, the last traces in both the plots correspond to V_{bg}= -225 V. A zero in the transconductance plot shows a plateau and peak is the riser in the conductance trace, based on these we explain the results in figure 7.16. It is noticed from the first trace at V_{bg}= 0 V in (a) that three subbands have been resolved, indicated by 1, 2, and 3; the 1 being the ground state. As the density of 1D electrons was reduced by increasing the back gate voltage all the higher energy plateaus smear out except the ground state which showed an interesting evolution of half-integer plateau at $0.5(2e^2/h)$ when the carrier density was sufficiently low as indicative in the last three traces in (a). A dotted black-line as a guide to the eye shows the evolution of $0.5(2e^2/h)$ as the density was reduced considerably. The effect of in-plane magnetic field is evident in (b). The first trace in (b) at V_{bg}=0 V shows the spin polarised subbands indicated by 0.5,

1, 1.5, 2,... in the multiples of $2e^2/h$ along with their spin orientations. It is assumed that $0.5(2e^2/h)$ is the spin-down $\downarrow$ state and $(2e^2/h)$ is spin-up $\uparrow$ state, and so on. As the back gate voltage was increased to $\sim$ - 62.5 V, an enhancement in the splitting of 1D subbands was observed. This may be noticed in a few traces below the trace marked by an asterisk symbol (*). As the density of 1D electrons was further reduced, a number of interesting events were noticed. For example, traces between the asterisk symbol (*) and the plus symbol (+) showed how the energy levels interact according to spin orientations as the density of the wire was reduced. It was realised that the 1 ($\uparrow$) interacted with the 1.5 ($\downarrow$) due to level crossing [133, 136] as the confinement/density was reduced resulting in smearing out of plateau at $2e^2/h$, as can been seen in the trace just below the plus (+) symbol. The traces above it reflect how the system was evolving to reach in the latter stage. It may also be noticed in this regime that the higher subbands such as 1.5($\downarrow$) and 2($\uparrow$) had already crossed before the effect was seen on the 1 ($\uparrow$) and 1.5 ($\downarrow$) [see, trace with plus (+) symbol]. On further reducing the carrier density the higher plateaus smeared out except the $0.5(2e^2/h)$ in the ground state and was found to get strengthened as the density was reduced.

Using the method described in section 7.3.1 and also suggested by Glazman and Larkin [137], the density of electrons was estimated in the weaker confinement to be $n_{2D} \sim 5.5 \times 10^{10} cm^{-2}$ where the e^2/h was observed in the conductance measurement at V_{sg}= -2.0 V and V_{bg}= -225 V [Figure 7.15]. For estimation of density of 1D electrons n_{1D} per unit length, the depletion length is $l \sim$ 135 nm of the 2DEG created by the split-gate [138] and using the relation $l = \epsilon\epsilon_0 V_P / 2\pi^2 n_{2D} e$, where $n_{2D} \sim 5.5 \times 10^{10} cm^{-2}$ (estimated above), and $V_P = V_{sg}$=-2 V. Using the value of l, n_{1D} was estimated such that the relation $n_{1D}\ a_B = 6.7 \times 10^{-3} \ll 1$,

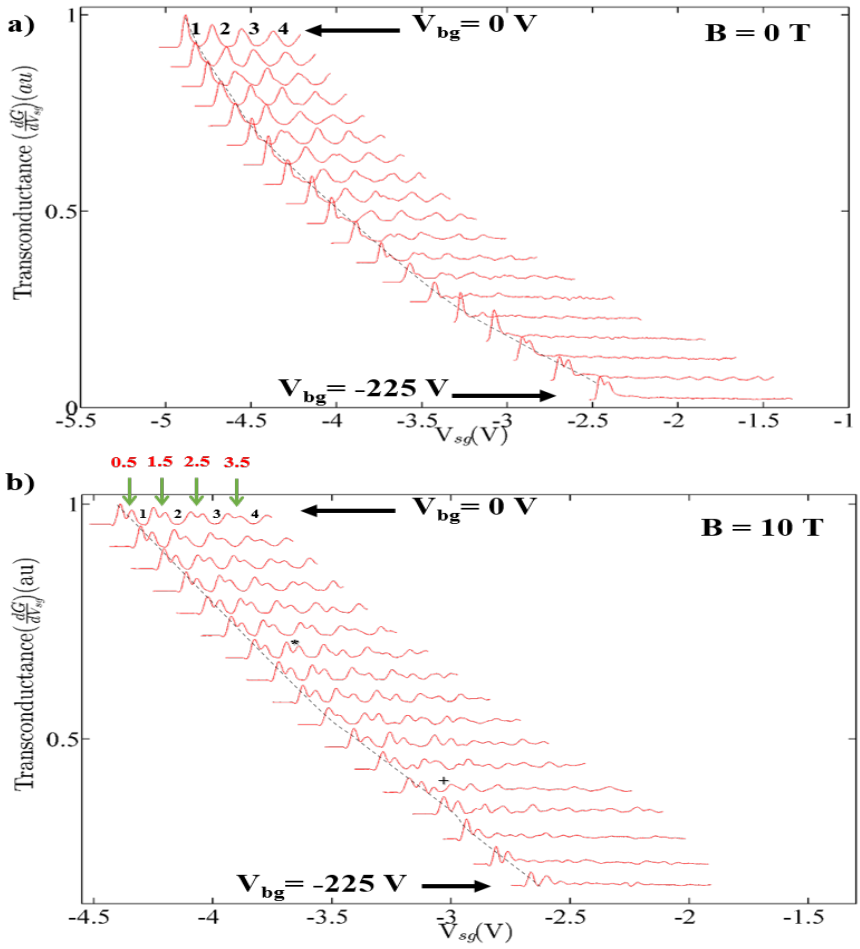

Figure 7.16: The transconductance (dG/dVsg) plots of the detailed conductance data, a part of which is shown in Fig. 3. Here, dG/dVsg is plotted as a function of Vsg and Vbg, the top trace is taken at V_{bg}=0 V, and subsequent traces were taken at increments of -12.5 V so that the last trace was taken at Vbg=-225 V. The plots have been offset vertically and horizontally for clarity. (a) dG/dV_{sg} Vs. V_{sg} plots when the back gate was made more negative, resulting in smearing out of conductance plateaus represented by valley in the transconductance peaks, and in the weaker confinement at a structure at e^2/h was seen which strengths at V_{bg}= -225 V, as shown by a green vertical arrow. b) the transconductance plots in the presence of in-plane magnetic field of 10 T. Spin splitting of 1D subbands due to Zeeman splitting is clearly visible as indicated by green, down arrows along with subbands indexing. On reducing the carrier density by making the back gate voltage more negative, a sequence of interaction effects were observed in traces between asterisk (*) and plus (+) symbols. On further lowering the density and the confinement potential, higher order plateaus smear out leaving a structure at e^2/h, which is strengthened compared to its counterpart in (a).

which is a requirement for the spin-incoherent transport [59–61].

In the case of a low density quantum wire such that $n_{1D} \ll 1/a_B$, the kinetic energy is small compared to the electron-electron interaction energy $e^2 n/\epsilon$, where a_B is the effective Bohr radius of GaAs ($a_B = \epsilon\hbar/m^* e^2$) and ϵ is dielectric constant of GaAs. Therefore, in the low density regime, the electrons can be considered as classical particles placed at equidistant positions to minimise the Coulomb repulsion. Such rearrangement of electrons in 1D is called Wigner lattice [18, 61, 132]. The 1D electrons forming a Wigner lattice can be viewed as forming anti-ferromagnetic Heisenberg spin chain with small exchange coupling, J between the nearest neighbours [58, 59, 139]. Such spin modes propagate independently to the charge modes, therefore their combined effect can affect the conductance in the ground state of such a quantum wire. The results in Figure 7.15 (b) where the $0.5(2e^2/h)$ fluctuates first in the moderate density regime and later strengthens in the low density regime could be an indicative of spin modes propagating with different velocity affecting the conductance in the ground state.

The major result in the this chapter by considering that spin modes are active in addition to the charge modes, so that the total conductance can be expressed as, $G = 1/(R_\rho + R_\sigma + R_s)$, where $R_\rho + R_\sigma + R_s$ are resistance contributions from charge, spin, and series resistance, respectively. Since R_s is the external resistance due to the leads, Ohmic contacts, etc. which can be accurately measured therefore, it is eliminated so that G depends on $R_\rho + R_\sigma$. It is known that the charge contribution is always $h/2e^2$ due to Büttiker formula [42], however, R_σ does not contribute to any resistance in the large density regime due to no exchange between the electrons therefore total G is equal to $2e^2/h$. At low density regimes, when $n_{1D} \ll 1/a_B$, the charge contribution to resistance remains the same ($h/2e^2$),

whereas spin excitations come into account due to exchange coupling J between the low density electrons due to Coulomb repulsive interactions between them, as given by $J \sim E_E(n_{1D}a_B)^{-3/4}exp(-\eta(n_{1D}a_B)^{-1/2})$, where E_F is Fermi energy of 2DEG, and $\eta \sim 2.82$ [59, 61]. It may be noted that J varies exponentially with n_{1D}, therefore the former becomes very significant at very low densities. Also, for a similar reason, estimation of J is very difficult due to inaccuracies in estimation of n_{1D}. Furthermore, the spin contribution to resistance becomes effective when $J \ll T \ll E_F$, the measurement temperature of 70 mK is well within this regime when $J/k_B \sim 2$ mK from [19], and $E_F/k_B \sim 47$ K (E_F= 4.1 meV for 2DEG). At high temperatures $> J/k_B$, due to the isotropic coupling of the spins, R_σ strengthens and saturates at $h/2e^2$ as theoretically derived in reference [59]. Therefore, total $G = 1/(\frac{h}{2e^2} + \frac{h}{2e^2}) = e^2/h$, which explains the results in the low-density regime of a quantum wire.

7.6 Summary

In this chapter a study of the quasi-1D quantum wires in a weakly-confined region where low electron density is achieved using a back gate. The weakly-confined region has strong electron-electron interactions as well as the possibility of exploring a spin-incoherent Luttinger liquid. Spin-incoherence is usually favoured at very low electron density. The evidence of the spin-incoherent Luttinger liquid was observed in the form of a conductance plateau at e^2/h and is accompanied by the disappearance of the plateau at $2e^2/h$. An in-plane magnetic-field dependence study was performed which showed the enhancement of the plateau at e^2/h as the magnetic field strength increased as well as the Zeeman splitting of the 1D

subbands. In addition at low density, spin polarised e^2/h was observed accompanied by the usual $2e^2/h$. Therefore, the present chapter deals with studies of observation of spin coherent i.e. intrinsic spin polarised e^2/h and spin incoherent e^2/h structure at low electron density.

Chapter 8

Conclusions

8.1 Summary

This chapter provides a summary of the chapters in this thesis which presents experiments of electron transport in quasi-1D quantum wires showing electron interaction effects. The key findings of the experimental chapters are summarised in this chapter as well as suggestions of additional work that can be continued in the future. The experimental results in this thesis provide an insight and advancement in the research of electron transport in quasi-1D wires.

Chapter 4 provides a detailed documentation of the fabrication process of making split-gates devices as well as the development of additional gates such as a mid-line gate, top gate and the back gate to make a systematic investigation of quasi-1D wires in the weak confinement regime. The fabrication techniques were iteratively refined to produce devices with low-resistance Ohmic contacts and high resolution electron beam lithography gate geometries. Those gate geometries allow the confinement of 1D wires to be tuned independently of the split-gates.

Chapter 5 shows results from a novel device consisting of split-gates as well as the patterning of thin mid-line gates of width of 60 nm in an attempt to create two lateral and closely separated 1D wires in a single 2DEG. The differential conductance measurements showed two 1D wires conducting as well as a mixing region in-between those wires. The mixing region showed an addition of both the wires to $4e^2/h$ which indicates that both 1D wires are uncoupled. The different regimes

of the differential conductance measurements were explored further by performing subband spectroscopy measurements using a dc-bias technique thus allowing the investigation of subband energies of the adjacent and mixed 1D wires. A detailed study was done to investigate the effect of perpendicular magnetic field on the mixing between the two 1D wires. The application of a perpendicular magnetic field localised the wavefunction of 1D wires thus reducing the overlapping of two 1D wires.

Asymmetric voltage bias was applied to the arms of the split-gates device to laterally shift the channel in +/- directions transverse to the current direction and it was used to probe the variation of potential in the channel. The experimental data confirmed that the creation of the two wires is by means of electrostatic effects only and not by an impurity in the channel. The dependence on density was investigated by controlled illumination of the device. The experimental results show that increasing the density enhances the coupling of the 1D wires and both 1D wires starts to anti-cross. This behaviour is consistent with a phenomenon of increasing the density in the 1D wire as more electrons are available to couple through the mid-line gate.

Chapter 6 presents an experimental study of coupled 1D wires in a single 2DEG showing wavefunction-coupling of the two 1D wires using a 20 nm thin mid-line gate. The differential conductance measurements showed two 1D wires conducting as well as a mixing region in-between those wires. The mixing region shows complicated mixing of the subbands of the 1D wire where a clear crossing is observed. A temperature dependant study was performed to confirm that distinct regions are created by the mid-line gate that are due to electrostatic confinement rather than electron interactions. The interaction effects between the two 1D

wires can be tuned from crossing to anti-crossing by laterally shifting the 1D channel using asymmetric voltage. The dc-conductance measurements performed showed clear distinct regions of both 1D wires and their mixing regime each with different subband energy spacing.

The last experimental chapter 7 presents an experimental study of the quasi-1D quantum wires in a weakly-confined region where low electron density is achieved using a back gate. The weakly-confined region has strong electron-electron interactions as well as the possibility of exploring a spin-incoherent Luttinger liquid. Spin-incoherence is usually favoured at very low electron density. The evidence of the spin-incoherent Luttinger liquid was observed in the form of a conductance plateau at e^2/h and is accompanied by the disappearance of the plateau at $2e^2/h$. An in-plane magnetic-field dependence study was performed which showed the enhancement of the plateau at e^2/h as the magnetic field strength increased as well as the Zeeman splitting of the 1D subbands. In addition at low density, spin polarised e^2/h was observed accompanied by the usual $2e^2/h$. Therefore, the present chapter deals with studies of observation of spin coherent i.e. intrinsic spin polarised e^2/h and spin incoherent e^2/h structure at low electron density in moderately longer wires of length 700-900 nm using a back gate device.

8.2 Further Work

Possible future works are discussed below where some of which may be pursued using the existing devices and measurement set-up while other ideas will only be possible with improvements in fabrication and measurement methods to produce

new and novel devices and experiments.

8.2.1 Back-Gated Devices

Using a back gate to control the density of the 2DEG produces a new range of confinement strengths. The addition of a back gate to the device can allow the variation of the density of the 2DEG as well as controlled illumination to produce a wide range of density.The device measured in the thesis was thinned to 50 μm and thinning the device further will produce a more profound change in the density of the 2DEG for a particular back gate voltage. The back-gate voltages required to deplete the 2DEG becomes less negative as the device becomes thinner. Instead of depositing an overall back gate as was done in this work, a patterned back-gate to produce a new range of confinement strengths can be investigated.

8.2.2 Double Quantum Well devices

Exploring double quantum well devices where strong coupling of wavefunctions of 1D wires can be explored further by independently tuning the density in each of the 2DEG separately. Selectively tuning the upper 2DEG can be achieved by adding a bar gate as well as a top gate. The lower 2DEG can be tuned by thinning the sample down using the method described in fabrication chapter 4 which can achieve a thickness of around 50 μm and depositing a patterned back gate. A schematic diagram of the proposed device is shown in figure 8.1 showing a split-gates device with a mid-line gate. The top gate could be used to control the density of the upper 2DEG while the back gate could be used to tune the

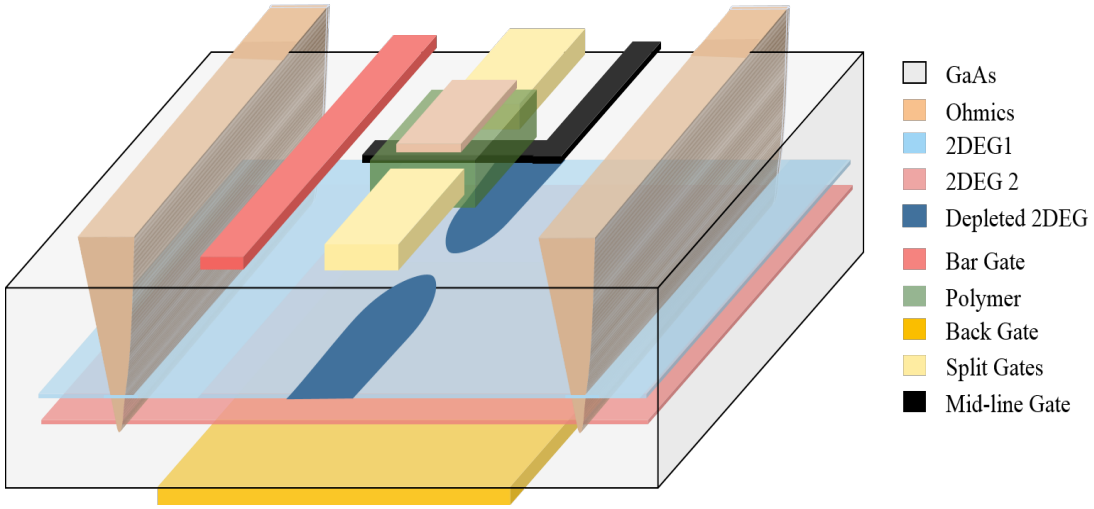

Figure 8.1: A 3D Schematic diagram of a split-gates device with independent control of mid-line, bar gate, top gate and back gate to control the density and selectivity delete the upper and lower 2DEG independently.

density of the lower 2DEG. It is suggested to perform transport measurement in longer 1D wires to investigate the interaction effects for possible spin phases. A detailed investigation could be carried out in the spin-incoherent regime and a temperature dependent set of measurements made which could not be extensively carried out in the present work may be taken up to understand the physics in the incoherent regime. It would be interesting to study the influence of RF on the incoherent electrons and performing NMR in the low density regimes.

8.2.3 Top-Gated Devices

Improving the top-gated devices is needed to give more precise control of the density and confinement potential of the 1D wire. This can be achieved by exploring different types of dielectrics materials other than the cross-linked PMMA. Dielectric materials with different k-dielectric values such as silicon dioxide, silicon

nitride and aluminium oxide can be used to create the top-gate. Reducing the screening and capacitive effects of the top-gate on the 1D wire could be reduced by optimising the thickness of dielectric layer deposited for the top-gate. Finally, wafers with much deeper 2DEG more than 300 nm could also be used which allows higher electron mobilities and shallower confinement of the quantum wire. In addition, complex gate geometries may be utilised to study the transport in weakly confined 1D wires especially longer wires whose physics is not yet fully understood.

Appendix A

A Wafer Growth Specifications

The growth matrices of the two GaAs/AlGaAs HEMT wafers used in this thesis are given below. The electron mobility and density were measured at 1.4 K in dark and in light after illumination using a red LED. The ratio of Al ,x, in $Al_xGa_{1-x}As$ is 0.33. The wafers were grown in an MBE system on a semi-insulating <100> gallium arsenide substrate in Cavendish Laboratory.

A.1 W0475

Layer	Material	Thickness	Si Doping (cm^{-3})	Comments
1	GaAs	10 nm	-	Cap layer
2	AlGaAs	40 nm	1.10×10^{16}	Doping layer
3	AlGaAs	40 nm	-	Spacer layer
4	GaAs	1000 nm	-	Buffer layer
5	GaAs	2.5 nm	-	Repeating 100 times
6	AlGaAs	2.5 nm	-	Repeating 100 times
7	AlAs	75 nm	-	
8	GaAs	50 nm	-	Smoothing layer
9	GaAs	500 μm	-	Semi-insulating substrate

Table A: Growth matrix of GaAs W0475 wafer

The carrier density of electron,n in the dark is 1.9×10^{11} cm^{-2} and the mobility of electron μ in the dark is 3.08×10^6 $cm^2V^{-1}s^{-1}$. The carrier density of electron,n

in the light is 3.40×10^{11} cm^{-2} and the mobility of electron μ in the light is 5.90×10^{6} cm^{2}V^{-1}s^{-1}.

A.2 W0731

Layer	Material	Thickness	Si Doping (cm^{-3})	Comments
1	GaAs	10 nm	-	Cap layer
2	AlGaAs	200 nm	-	Un-doped spacer layer
3	GaAs	0.56 nm	-	
4	As:Si	-	8.00×10^{11}	Si "Delta" doping
5	GaAs	0.56 nm	-	
6	AlGaAs	75 nm	-	Un-doped spacer layer
7	GaAs	1000 nm	-	Buffer Layer
8	GaAs	500 μm	-	Semi-insulating substrate

Table B: Growth matrix of GaAs W0731 wafer

The carrier density of electron,n in the dark is 4.5×10^{10} cm^{-2} and the mobility of electron μ in the dark is 1.23×10^{6} cm^{2}V^{-1}s^{-1}. The carrier density of electron,n in the light is 2.20×10^{11} cm^{-2} and the mobility of electron μ in the light is 7.95×10^{6} cm^{2}V^{-1}s^{-1}.

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